19-4817; Rev 1; 9/10

EVALUATION KIT AVAILABLE

High-Frequency, Low-Cost SMBus Chargers

General Description

The MAX17435/MAX17535 integrated multichemistry battery-charger ICs simplify construction of accurate and efficient chargers. The MAX17435/MAX17535 provide SMBus™-programmable charge current, charge voltage, input current limit, relearn voltage, and digital readback of the IINP voltage. The MAX17435/MAX17535 utilize a charge pump to control the adapter selection n-channel MOSFETs when the adapter is present. When the adapter is absent, the charge pump is shut down and a p-channel MOSFET selects the battery.

The MAX17435/MAX17535 provide up to 7A of charge current to 2, 3, or 4 lithium-ion (Li+) cells in series. The charge current, and input current-limit sense amplifiers have low offset errors and can use 10mΩ sense resistors. The MAX17435/MAX17535 fixed-inductor ripple architecture significantly reduces component size and circuit cost.

The MAX17435/MAX17535 provide a digital output that indicates the presence of the adapter, an analog output that indicates the adapter or battery current, depending upon the presence or absence of the adapter, and a digital output that indicates when the adapter current exceeds a user-defined threshold.

The MAX17435 switches at an 850kHz frequency and the MAX17535 switches at 500kHz.

The MAX17435/MAX17535 are available in a small, 4mm x 4mm x 0.75mm, 24-pin, lead-free TQFN package. An evaluation kit is available.

Applications

Notebook Computers

PDAs and Mobile Communicators

2- to 4- Li+ Cell Battery-Powered Devices

SMBus is a trademark of Intel Corp.

Features

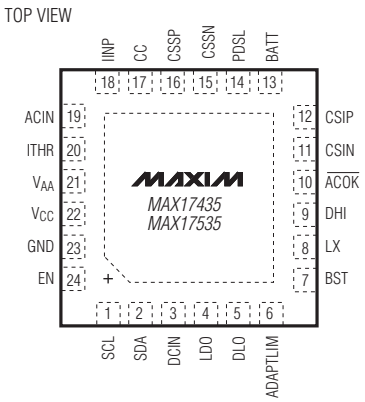
- **Low-Cost SMBus Charger**
- **High Switching Frequency (0.85MHz/0.5MHz)**
- **Internal Boost Switches**
- **SMBus-Programmable Charge Voltage, Input Current Limit, Charge Current, Relearn Voltage, and Digital IINP Readback**
- **Single-Point Compensation**
- **Automatic Selection of System Power Source**
  - **Adapter n-Channel MOSFETs Driven by an Internal Dedicated Charge Pump**
  - **Adapter Soft-Start**
- **±0.4% Accurate Charge Voltage**
- **±2.5% Accurate Input Current Limiting**
- **±3% Accurate Charge Current**
- **Monitor Outputs for**
  - **AC Adapter Current (±2% Accuracy)**
  - **Battery Discharge Current (±2% Accuracy)**
  - **AC Adapter Presence**
- **AC Adapter Overvoltage Protection**
- **11-Bit Battery Voltage Setting**
- **6-Bit, Charge-Current Setting/Input Current Setting**
- **Improved IINP Accuracy at Low Input Current**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17435ETG+	-40°C to +85°C	24 TQFN-EP*
MAX17535ETG+	-40°C to +85°C	24 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Pin Configuration



High-Frequency, Low-Cost SMBus Chargers

ABSOLUTE MAXIMUM RATINGS

DCIN, CSSP, BATT, CSIP to GND ..... -0.3V to +28V
CSIP to CSIN, CSSP to CSSN ..... -0.3V to +0.3V
V_{CC}, SCL, SDA, $\overline{V_{AA}}$, EN, ACIN, ITHR, ADAPTLIM, $\overline{ACOK}$ to GND ..... -0.3V to +6V
PDSL to GND ..... -0.3V to +37V
GND to PGND ..... -0.3V to +0.3V
DHI to LX ..... -0.3V to (V_{BST} + 0.3V)
BST to LX ..... -0.3V to +6V
BST to GND ..... -0.3V to +34V
DLO to PGND ..... -0.3V to (V_{LDO} + 0.3V)
LX to GND ..... -6V to +28V
CC, IINP to GND ..... -0.3V to (V_{LDO} + 0.3V)
LDO Short Circuit to GND ..... Momentary
Continuous Power Dissipation (T_A = +70°C)
24-Pin TQFN (derate 20.8mW/°C above +70°C) 1666mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, no load on LDO, V_{DCIN} = V_{CSSP} = V_{CSSN} = 19V, V_{LX} = 0V, V_{BST} - V_{LX} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 16.8V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLIES							
Adapter Present Quiescent Current (Note 1)		I_{DCIN} + I_{CSSP} + I_{CSSN}	Charging enabled, $V_{ADAPTER}$ = 19V, $V_{BATTERY}$ = 16.8V		3	6	mA
			Charging disabled		1.5	2.2	mA
BATT + CSIP + CSIN + LX Input Current		V_{BATT} = 16.8V	Adapter absent or charger shut down (Note 1)			2.0	µA
		V_{BATT} = 2V to 19V, adapter present (Note 1)			200	650	
DCIN Input Current	I_{DCIN}	Charger disabled			0.7	1.0	mA
V_{CC} Supply Current	I_{CC}	Charger added			1.5	2.5	mA
DCIN Input Voltage Range for Charger				8		26	V
DCIN Undervoltage-Lockout Trip Point for Charger		V_{DCIN} falling		7	7.2		V
		V_{DCIN} rising			7.7	7.9	
DCIN Input Voltage Range				8		26	V
CHARGE-VOLTAGE REGULATION							
Battery Full-Charge Voltage and Accuracy		ChargingVoltage() = 0x41A0		16.733	16.8	16.867	V
				-0.4		+0.4	%
		ChargingVoltage() = 0x3130		12.516	12.592	12.668	V
				-0.6		+0.6	%
		ChargingVoltage() = 0x20D0		8.333	8.4	8.467	V
				-0.8		+0.8	%
		ChargingVoltage() = 0x1060		4.15	4.192	4.234	V
				-1.0		+1.0	%
Battery Undervoltage-Lockout Trip Point for Trickle Charge				3	3.5	4	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO, V_{DCIN} = V_{CSSP} = V_{CSSN} = 19V, V_{LX} = 0V, V_{BST} - V_{LX} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 16.8V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGE-CURRENT REGULATION						
CSIP-to-CSIN Full-Scale Current-Sense Voltage			78.22	80.64	83.06	mV
Charge Current and Accuracy		RS2 = 10mΩ, Figure 1, ChargingCurrent() = 0x1f80	7.822	8.064	8.306	A
			-3		+3	%
		RS2 = 10mΩ, Figure 1, ChargingCurrent() = 0x0f80	3.829	3.968	4.107	A
			-3.5		+3.5	%
		RS2 = 10mΩ, Figure 1, ChargingCurrent() = 0x0080	64	128	192	mA
			-50		+50	%
Charge-Current Gain Error		Based on ChargeCurrent() = 128mA and 8.064A	-2		+2	%
INPUT CURRENT REGULATION						
Input Current-Limit Threshold		RS1 = 10mΩ, Figure 1, InputCurrent() = full scale	107.25	110	112.75	mV
			-2.5		+2.5	
		RS1 = 10mΩ, Figure 1, InputCurrent() = 0C80	62.08	64	65.92	
			-3		+3	
		RS1 = 10mΩ, Figure 1, InputCurrent() = 0780	36.86	38.4	39.94	%
			-4		+4	
CSSP/CSSN Input Voltage Range			8		26	V
IINP Voltage Gain			19.7	20	20.3	V/V
IINP Output Voltage Range			0		4.2	V
IINP Accuracy		V_{CSSP} - V_{CSSN} = 110mV	-5		+5	%
		V_{CSSP} - V_{CSSN} = 55mV	-4		+4	
		V_{CSSP} - V_{CSSN} = 5mV	-10		+10	
IINP Gain Error		Based on V_{CSSP} - V_{CSSN} = 110mV and V_{CSSP} - V_{CSSN} = 55mV	-1.5		+1.5	%
IINP Offset Error		Based on V_{CSSP} - V_{CSSN} = 110mV and V_{CSSP} - V_{CSSN} = 55mV	-350		+350	µV
REFERENCE						
REF Output Voltage	REF	I_{REF} = 50µA	4.082	4.096	4.115	V
REF Undervoltage-Lockout Threshold		REF falling		3.1	3.9	V
LINEAR REGULATOR						
LDO Output Voltage	LDO	I_{REF} = 50µA	5.2	5.4	5.6	V
LDO Load Regulation		0 < I_{LDO} < 40mA		127	250	mV
LDO Undervoltage-Lockout Threshold		LDO falling, 500mV (typ) hysteresis	3.2	4.1	5.0	V

High-Frequency, Low-Cost SMBus Chargers

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO, V_{DCIN} = V_{CSSP} = V_{CSSN} = 19V, V_{LX} = 0V, V_{BST} - V_{LX} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 16.8V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{ACOK}$						
$\overline{ACOK}$ Sink Current		V_{ACOK} = 0.4V, V_{ACIN} = 2.5V	1			mA
$\overline{ACOK}$ Leakage Current		V_{ACOK} = 5.5V, V_{ACIN} = 0.5V, T_A = +25°C			1	µA
ACIN						
ACIN Threshold		Rising, 20mV (typ) hysteresis	1.465	1.485	1.53	V
ACIN Input Bias Current		T_A = +25°C	-1		+1	µA
ITHR/ADAPTLIM						
ITHR Leakage Current		V_{ITHR} = 0V to LDO, T_A = +25°C	-1		+1	µA
ADAPTLIM Sink Current		V_{ITHR} > V_{IINP}	1			mA
ADAPTLIM Leakage Current		V_{ITHR} < V_{IINP}, T_A = +25°C			1	µA
ITHR Threshold		Calculated = V_{ITHR} - V_{IINP}	-12		+12	mV
LOGIC LEVELS						
SDA/SCL Input Low Voltage					0.8	V
SDA/SCL Input High Voltage			2.1			V
SDA/SCL Input Bias Current		T_A = +25°C	-1		+1	µA
SWITCHING REGULATOR						
DHI Off-Time K Factor		V_{DCIN} = 19V, V_{BATT} = 10V, MAX17435	55	61	67	ns/V
		V_{DCIN} = 19V, V_{BATT} = 10V, MAX17535	93	100	107	
Sense Voltage for Minimum Discontinuous Mode Ripple Current		V_{CSIP} - V_{CSIN}		5		mV
Zero-Crossing Comparator Threshold		V_{CSIP} - V_{CSIN}		5		mV
Cycle-by-Cycle Current-Limit Sense Voltage		V_{CSIP} - V_{CSIN}	120	125	130	mV
DHI Resistance High		I_{DHI} = 10mA		1.5	3	Ω
DHI Resistance Low		I_{DHI} = -10mA		0.8	1.6	Ω
DLO Resistance High		I_{DLO} = 10mA		3	6	Ω
DLO Resistance Low		I_{DLO} = -10mA		3	6	Ω
ADAPTER DETECTION						
Adapter Absence Detect Threshold		V_{DCIN} - V_{BATT}, V_{DCIN} falling	50	120	200	mV
Adapter Detect Threshold		V_{DCIN} - V_{BATT}, V_{DCIN} rising	340	430	600	mV
CHARGE-PUMP MOSFET DRIVER						
PDSL Gate-Driver Source Current		V_{PDSL} - V_{DCIN} = 3V, V_{DCIN} = 19V	40	64		µA
PDSL Gate-Driver Output Voltage HIGH		V_{DCIN} = 19V, open load	V_{DCIN} + 5.3	V_{DCIN} + 8		V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO, V_{DCIN} = V_{CSSP} = V_{CSSN} = 19V, V_{LX} = 0V, V_{BST} - V_{LX} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 16.8V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADAPTER OVERVOLTAGE PROTECTION						
ACOVP Threshold		Rising	2.04	2	2.1	V
ACOVP Threshold Hysteresis				30		mV
ADAPTER OVERCURRENT PROTECTION						
ACOCP Threshold		With respect to V_{CSSP} - V_{CSSN}		144		mV
ACOCP Blanking Time				16		ms
ACOCP Waiting Time		When ACOCP comparator is high and at the time the blanking time expires		0.6		s
PDSL SWITCH CONTROL						
PDSL Turn-Off Resistance				2.5	4	kΩ
SMBus TIMING SPECIFICATIONS						
SMBus Frequency	f_{SMB}		10		100	kHz
Bus Free Time	t_{BUF}		4.7			µs
START Condition Hold Time from SCL	$t_{HD:STA}$		4			µs
START Condition Setup Time from SCL	$t_{SU:STA}$		4.7			µs
STOP Condition Setup Time from SCL	$t_{SU:STO}$		4			µs
Holdup Time from SCL	$t_{HD:DAT}$		300			ns
Setup Time from SCL	$t_{SU:DAT}$		250			ns
SCL Low Period	t_{LOW}		4.7			µs
SCL High Period	t_{HIGH}		4			µs
Maximum Charging Period Without a Charge_Voltage() or ChargeCurrent() Command			140	175	210	s

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, no load on LDO, V_{DCIN} = V_{CSSP} = V_{CSSN} = 19V, V_{LX} = 0V, V_{BST} - V_{LX} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 16.8V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
INPUT SUPPLIES						
Adapter Present Quiescent Current		I_{DCIN} + I_{CSSP} + I_{CSSN} (Note 1)	Charging enabled, $V_{ADAPTER}$ = 19V, $V_{BATTERY}$ = 16.8V		6	mA
			Charging disabled		2.2	mA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO, V_{DCIN} = V_{CSSP} = V_{CSSN} = 19V, V_{LX} = 0V, V_{BST} - V_{LX} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 16.8V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
BATT + CSIP + CSIN + LX Input Current		V_{BATT} = 16.8V, Adapter absent or charger shut down (Note 1)		1.5	µA
		V_{BATT} = 2V to 19V, adapter present (Note 1)		650	
DCIN Input Current	I_{DCIN}	Charger disabled		1	mA
V_{CC} Supply Current	I_{CC}	Charger enabled		2.5	mA
DCIN Input Voltage Range for Charger			8	26	V
DCIN Undervoltage-Lockout Trip Point for Charger		V_{DCIN} falling	7		V
		V_{DCIN} rising		7.9	
DCIN Input Voltage Range			8	26	V
CHARGE-VOLTAGE REGULATION					
Battery Full-Charge Voltage and Accuracy		ChargingVoltage() = 0x41A0	16.73	16.87	V
			-0.416	+0.416	%
		ChargingVoltage() = 0x3130	12.516	12.668	V
			-0.6	+0.6	%
		ChargingVoltage() = 0x20D0	8.333	8.467	V
			-0.8	+0.8	%
		ChargingVoltage() = 0x1060	4.15	4.234	V
			-1.0	+1.0	%
Battery Undervoltage-Lockout Trip Point for Trickle Charge			3	4	V
CHARGE-CURRENT REGULATION					
CSIP-to-CSIN Full-Scale Current-Sense Voltage			78.22	83.06	mV
Charge Current and Accuracy		RS2 = 10mΩ, Figure 1, ChargingCurrent() = 0x1f80	7.822	8.306	A
			-3	+3	%
		RS2 = 10mΩ, Figure 1, ChargingCurrent() = 0x0f80	3.829	4.107	A
			-3.5	+3.5	%
		RS2 = 10mΩ, Figure 1, ChargingCurrent() = 0x0080	64	192	mA
			-50	+50	%
Charge-Current Gain Error		Based on ChargeCurrent() = 128mA and 8.064A	-2	+2	%

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO, V_{DCIN} = V_{CSSP} = V_{CSSN} = 19V, V_{LX} = 0V, V_{BST} - V_{LX} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 16.8V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
INPUT CURRENT REGULATION					
Input Current-Limit Threshold		RS1 = 10mΩ, Figure 1, InputCurrent() = full scale	106.7	113.3	mV
			-2.5	+2.5	%
		RS1 = 10mΩ, Figure 1, InputCurrent() = 0C80	62.08	65.92	mV
			-3	+3	%
		RS1 = 10mΩ, Figure 1, InputCurrent() = 0780	36.86	39.94	mV
			-4	+4	%
CSSP/CSSN Input Voltage Range			8	26	V
IINP Voltage Gain			19.7	20.3	%
IINP Output Voltage Range			0	4	V
IINP Accuracy		V_{CSSP} - V_{CSSN} = 110mV	-5	+5	%
		V_{CSSP} - V_{CSSN} = 55mV	-4	+4	
		V_{CSSP} - V_{CSSN} = 5mV	-11	+11	
IINP Gain Error		Based on V_{CSSP} - V_{CSSN} = 100mV and V_{CSSP} - V_{CSSN} = 20mV	-1.5	+1.5	%
IINP Offset Error		Based on V_{CSSP} - V_{CSSN} = 100mV and V_{CSSP} - V_{CSSN} = 5mV	-520	+520	µV
REFERENCE					
REF Output Voltage	REF	I_{REF} = 50µA	4.075	4.115	V
REF Undervoltage-Lockout Threshold		REF falling		3.9	V
LINEAR REGULATOR					
LDO Output Voltage	LDO	I_{REF} = 50µA	5.2	5.6	V
LDO Load Regulation		0 < I_{LDO} < 40mA		300	mV
LDO Undervoltage-Lockout Threshold		LDO falling, 500mV (typ) hysteresis	3.2	5.0	V
$\overline{ACOK}$					
$\overline{ACOK}$ Sink Current		V_{ACOK} = 0.4V, V_{ACIN} = 1.5V	1		mA
ACIN					
ACIN Threshold		Rising, 20mV (typ) hysteresis	1.465	1.530	V
ACIN Input Bias Current			-1	+1	µA
ITHR/ADAPTLIM					
ITHR Leakage Current		V_{ITHR} = 0 to 5.4V		1	µA
ADAPTLIM Sink Current		V_{ITHR} > V_{IINP}	1		mA
ADAPTLIM Leakage Current		V_{ITHR} < V_{IINP}		1	µA
ITHR Threshold		Calculated = V_{ITHR} - V_{IINP}	-12	+12	mV

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO, V_{DCIN} = V_{CSSP} = V_{CSSN} = 19V, V_{LX} = 0V, V_{BST} - V_{LX} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 16.8V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
LOGIC LEVELS					
SDA/SCL Input Low Voltage				0.8	V
SDA/SCL Input High Voltage			2.1		V
SDA/SCL Input Bias Current			-1		µA
SWITCHING REGULATOR					
DHI Off-Time K Factor		V_{DCIN} = 19V, V_{BATT} = 10V, MAX17435	55	67	ns/V
		V_{DCIN} = 19V, V_{BATT} = 10V, MAX17435	93	107	
Cycle-by-Cycle Current-Limit Sense Voltage		V_{CSIP} - V_{CSIN}	120	130	mV
DHI Resistance High		I_{DHI} = 10mA		3	Ω
DHI Resistance Low		I_{DHI} = -10mA		1.6	Ω
DLO Resistance High		I_{DLO} = 10mA		6	Ω
DLO Resistance Low		I_{DLO} = -10mA		6	Ω
ADAPTER DETECTION					
Adapter Absence Detect Threshold		V_{DCIN} - V_{BATT}, V_{DCIN} falling	50	200	mV
Adapter Detect Threshold		V_{DCIN} - V_{BATT}, V_{DCIN} rising	270	600	mV
CHARGE-PUMP MOSFET DRIVER					
PDSL Gate-Driver Source Current		V_{PDSL} - V_{DCIN} = 3V, V_{DCIN} = 19V	40		µA
PDSL Gate-Driver Output Voltage High		V_{DCIN} = 19V	V_{DCIN} + 5.3		V
ADAPTER OVERVOLTAGE PROTECTION					
ACOVP Threshold		Rising	2.04	2.1	V
PDSL SWITCH CONTROL					
PDSL Turn-Off Resistance				4	kΩ
SMBus TIMING SPECIFICATIONS					
SMBus Frequency	f_{SMB}		10	100	kHz
Bus Free Time	t_{BUF}		4.7		µs
START Condition Hold Time from SCL	$t_{HD:STA}$		4		µs
START Condition Setup Time from SCL	$t_{SU:STA}$		4.7		µs
STOP Condition Setup Time from SCL	$t_{SU:STO}$		4		µs

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO, V_{DCIN} = V_{CSSP} = V_{CSSN} = 19V, V_{LX} = 0V, V_{BST} - V_{LX} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 16.8V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Hold Time from SCL	$t_{HD:DAT}$		300		ns
Setup Time from SCL	$t_{SU:DAT}$		250		ns
SCL Low Period	t_{LOW}		4.7		µs
SCL High Period	t_{HIGH}		4		µs
Maximum Charging Period Without a Charge_Voltage() or ChargeCurrent() Command		(Note 4)	140	210	s

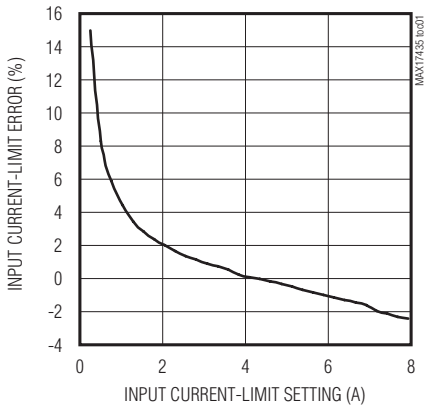
Note 1: Adapter present conditions are tested at V_{DCIN} = 19V and V_{BATT} = 16.8V. Adapter absent conditions are tested at V_{DCIN} = 16V, V_{BATT} = 16.8V.

Note 2: Specifications to T_A = -40°C are guaranteed by design and not production tested.

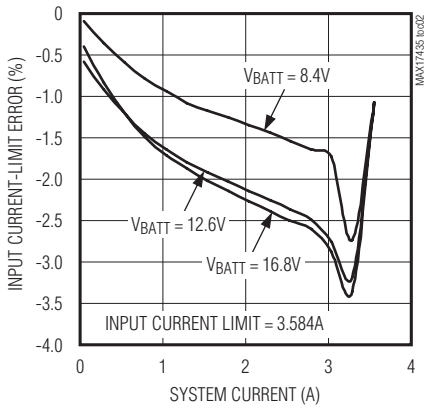
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 19V, V_{CC} = V_{DD} = 5V, EN = V_{CC}, T_A = +25°C, unless otherwise specified.)

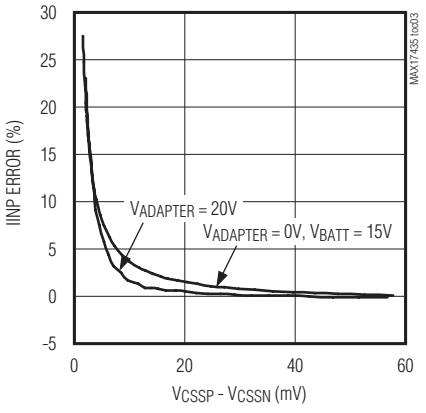
INPUT CURRENT-LIMIT ERROR vs. INPUT CURRENT-LIMIT SETTING



INPUT CURRENT-LIMIT ERROR vs. SYSTEM CURRENT



IINP ERROR vs. SYSTEM CURRENT (DC SWEEP)

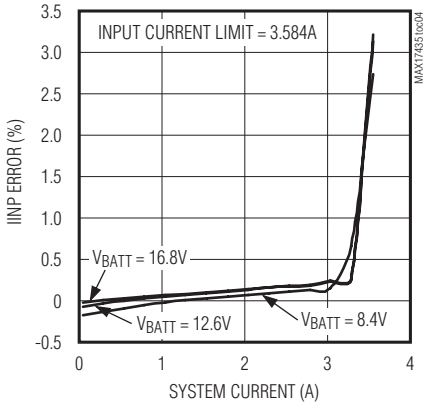


High-Frequency, Low-Cost SMBus Chargers

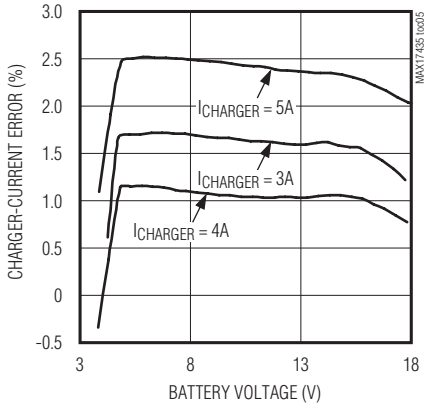
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 19V, V_{CC} = V_{DD} = 5V, EN = V_{CC}, T_A = +25°C, unless otherwise specified.)

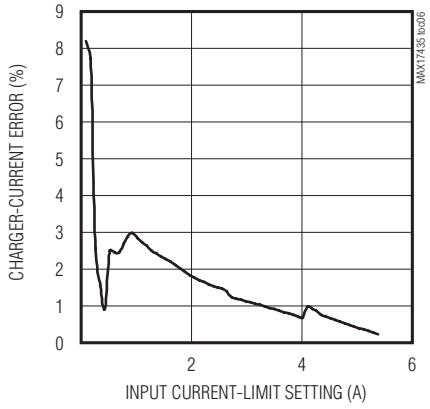
IINP ERROR vs. SYSTEM CURRENT



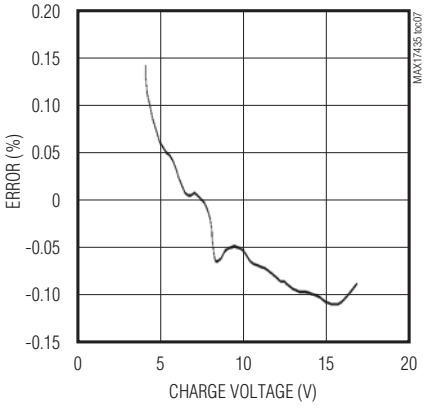
CHARGER-CURRENT ERROR vs. BATTERY VOLTAGE



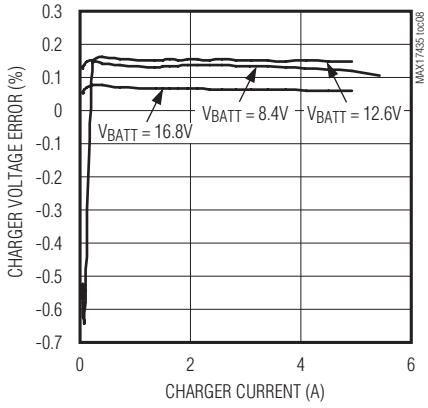
CHARGER-CURRENT ERROR vs. SMBus SETTING



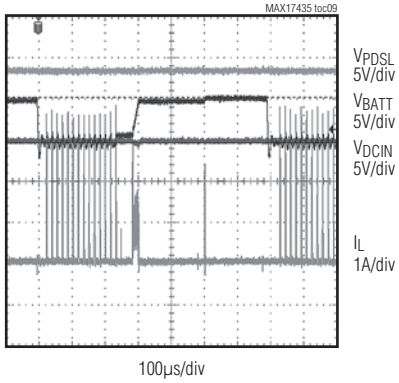
CHARGE VOLTAGE ACCURACY AT 3.854A



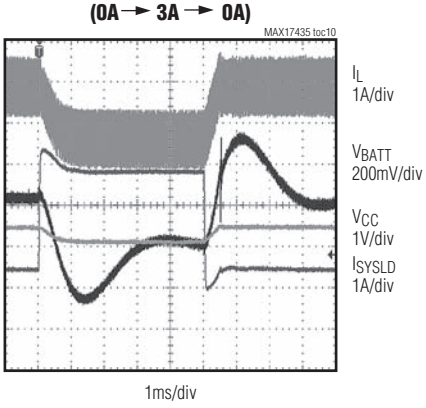
CHARGER VOLTAGE ERROR vs. CHARGER CURRENT



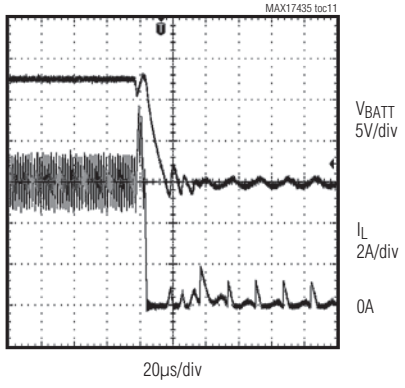
BATTERY REMOVAL (V_{BATT} = 3V)



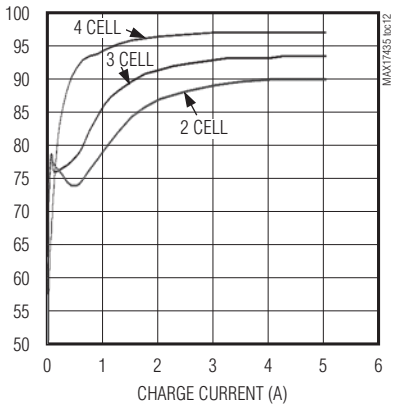
SYSTEM LOAD TRANSIENT (0A → 3A → 0A)



CHARGE-OUTPUT SHORT CIRCUIT



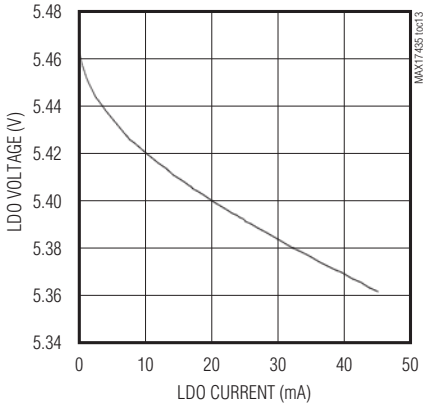
EFFICIENCY vs. CHARGE CURRENT (2, 3, AND 4 CELLS)



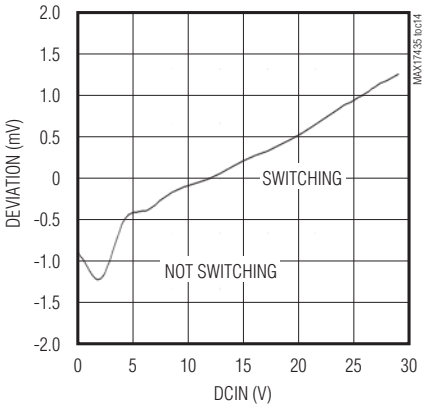
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 19V, V_{CC} = V_{DD} = 5V, EN = V_{CC}, T_A = +25°C, unless otherwise specified.)

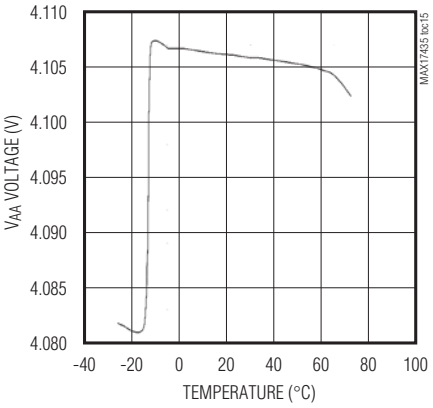
LDO VOLTAGE vs. LDO CURRENT



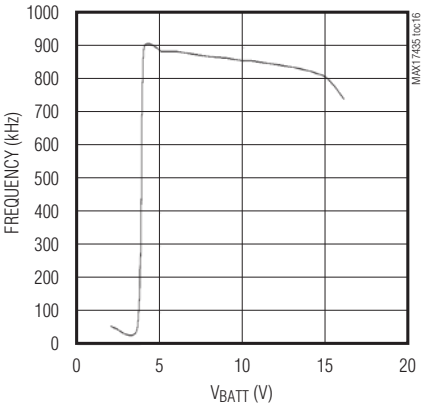
V_{AA} DEVIATION, SWITCHING AND NOT SWITCHING



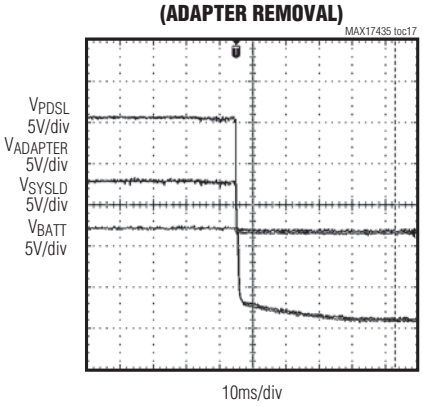
V_{AA} vs. TEMPERATURE



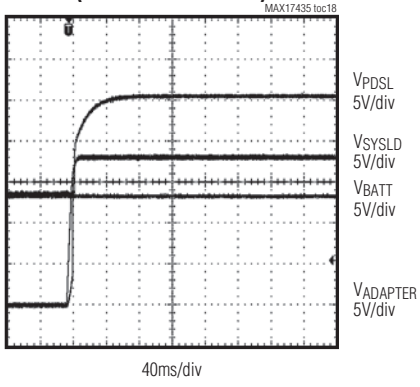
FREQUENCY vs. V_{BATT} AT 4A I_{CHG}



POWER-SOURCE SELECTOR SCHEME WITH BATTERY PRESENT (ADAPTER REMOVAL)



POWER-SOURCE SELECTOR SCHEME WITH BATTERY PRESENT (ADAPTER INSERTION)



High-Frequency, Low-Cost SMBus Chargers

Pin Description

PIN	NAME	FUNCTION
1	SCL	SMBus Clock Input. Connect to an external pullup resistor according to SMBus specifications.
2	SDA	SMBus Data I/O. Open-drain output. Connect to an external pullup resistor according to SMBus specifications.
3	DCIN	Charger Supply Input. Connect to adapter supply. For minimum input bias current connect to the center of the input/soft-start FETs. Bypass with a 1µF ceramic capacitor to PGND placed close to the pin. Add a 10Ω resistor to reduce input surge at adapter insertion.
4	LDO	Linear Regulator Output. This is a 30mA LDO that powers the DLO driver, the BST circuit, and the internal SMBus circuitry. Bypass with a 1µF ceramic capacitor to PGND placed close to the pin. LDO is active when the Adapter Present = 1, independent of the state of EN. LDO is also active when DCIN is supply by the battery while Adapter Present = 0 and EN is high. The SMBus registers are reset by the rising LDO UVLO.
5	DLO	Low-Side Power-MOSFET Driver Output. Connect to low-side n-channel MOSFET gate.
6	ADAPTLIM	Adaptive System Current-Limit Comparator Output. This open-drain output is high impedance when the voltage at the IINP pin is lower than the ITHR threshold. For a typical application, use a 10kΩ pullup resistor to LDO (pin 4).
7	BST	High-Side Driver Supply. Connect a 0.1µF capacitor from BST to LX.
8	LX	High-Side Driver Source Connection
9	DHI	High-Side Power MOSFET Driver Output. Connect to high-side n-channel MOSFET gate.
10	$\overline{\text{ACOK}}$	AC Detect Output. This open-drain output is high impedance when ACIN is lower than 1.485V. The $\overline{\text{ACOK}}$ output remains high when the MAX17435/MAX17535 are powered down. For a typical application, use a 10kΩ pullup resistor to LDO (pin 4).
11	CSIN	Output Current-Sense Negative Input. Connect this pin to the negative terminal of the sense resistor. See the *Setting Charge Current* section for resistor value and scaling.
12	CSIP	Output Current-Sense Positive Input. Connect a current-sense resistor from CSIP to CSIN; the voltage across these two pins is interpreted by the MAX17435/MAX17535 as proportional to the charge current delivered to the battery with approximately 110mV full-scale voltage. See the *Setting Charge Current* section for resistor value and scaling.
13	BATT	Battery Voltage Feedback Input. Connect as close as possible to the battery terminal.
14	PDSL	Power-Source n-Channel MOSFET Switch Driver Output. When the adapter is not present or an overvoltage event is detected at the input, the PDSL output is pulled to GND with a 2.5kΩ (typ) resistor. Otherwise, it is typically 8V above the adapter voltage when the part is not using the battery. This is powered by an internal charge pump.
15	CSSN	Input Current-Sense Negative Input. See the description of the CSSP pin for resistor value and scaling.

Pin Description (continued)

PIN	NAME	FUNCTION
16	CSSP	Current Sense for Positive Input. Connect a current-sense resistor from CSSP to CSSN. The voltage across CSSP to CSSN determines the current at which the charger reduces charging current to keep from drawing more current from the adapter than is allowed. As the system current flowing in the resistor from CSSN to CSSP increases, the charger reduces charge current to keep the system current at the limit value. When the system current reaches 130% of InputCurrent() setting for more than 16ms, the PDSL pin turns off the adapter selector FET to prevent excess current from being drawn from the adapter. The adaptor selector FET is re-enabled after 0.6s. If the fault continues, the cycle is repeated three times after which the MAX17435/MAX17535 is latched off. To reset the latch, remove and reinsert the adapter.
17	CC	Voltage Regulation Loop-Compensation Point. Connect a 10nF capacitor from CC to GND.
18	IINP	Input Current-Monitor Output. The voltage at the IINP pin is 20 times the voltage from CSSP to CSSN. This voltage is present when charging is enabled to monitor the system current, and when the battery is discharging to monitor the battery discharge current.
19	ACIN	AC Adapter-Detect Input. ACIN is the input to a comparator with a 1.485V (typ) reference voltage. The output of the comparator is $\overline{ACOK}$. $\overline{ACOK}$ goes low when the threshold voltage is exceeded, indicating that the AC adapter is present, and it enables the charger. When the ACIN input is above 2.0V, the MAX17435/MAX17535 interpret that as an adapter overvoltage event. The charger is then disabled and the adapter MOSFETs are turned off. If the part is charging and the ACIN voltage drops below the programmed threshold, the charger is disabled, and a ChargeCurrent() and ChargeVoltage() command have to be written over the SMBus to re-enable the charger.
20	ITHR	Adaptive System Current-Limit Comparator Threshold. This pin connects to the inverting input of a comparator. The noninverting input of the comparator is the IINP input, while the output is driving the ADAPTLIM open drain. When the input to ITHR is greater than IINP, the ADAPTLIM output is high.
21	V_{AA}	4.096V Internal Reference Voltage; No External Load Allowed. Bypass to analog ground using a 1µF or greater ceramic capacitor. V_{AA} is active only after LDO and the internal reference are active.
22	V_{CC}	Circuitry Supply-Voltage Input. Connect to LDO through 10Ω and bypass with a 0.1µF capacitor to GND as close as possible to the package pin.
23	GND	Analog Ground
24	EN	Enable/Disable Charger Operation. This disables the charger and associated circuitry when EN goes low and is in addition to the $\overline{ACOK}$ charger enable. If the adapter is absent and EN is pulled up to a voltage higher than 2.4V, LDO, V_{AA}, the input charge current, and the battery discharge current monitor on IINP are enabled.
—	EP	Exposed Pad. Connect backside EP to power ground.

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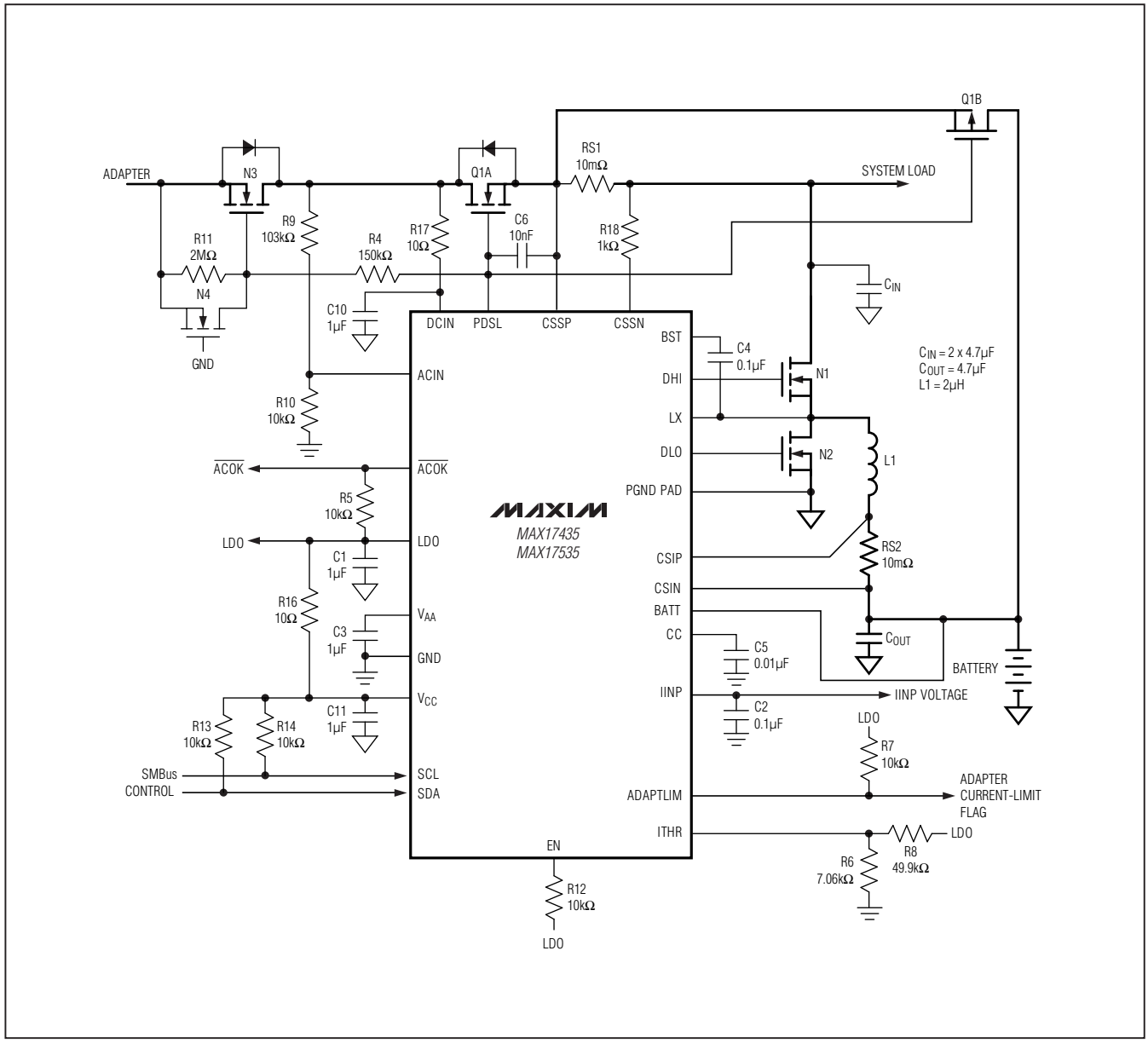

Figure 1. Standard Application Circuit

Detailed Description

The MAX17435/MAX17535 charger includes all the functions necessary to charge Li+, NiMH, and NiCd smart batteries. A high-efficiency synchronous rectified step-down DC-DC converter is used to implement a constant-current constant-voltage charger. The DC-DC converter drives a high-side n-channel MOSFET and provides synchronous rectification with a low-side n-channel MOSFET. The charge current and input current-sense amplifiers have low-input offset errors (200µV typ), allowing the use of small-valued sense resistors. The MAX17435/MAX17535 use an SMBus interface similar to the MAX8731A to set charge current, charge voltage, and input current limit. In addition, the MAX17435/MAX17535 SMBus interface supports ChargeVoltage (), ChargeCurrent(), InputCurrent(), RELEARN(), and IINPVoltage() readback.

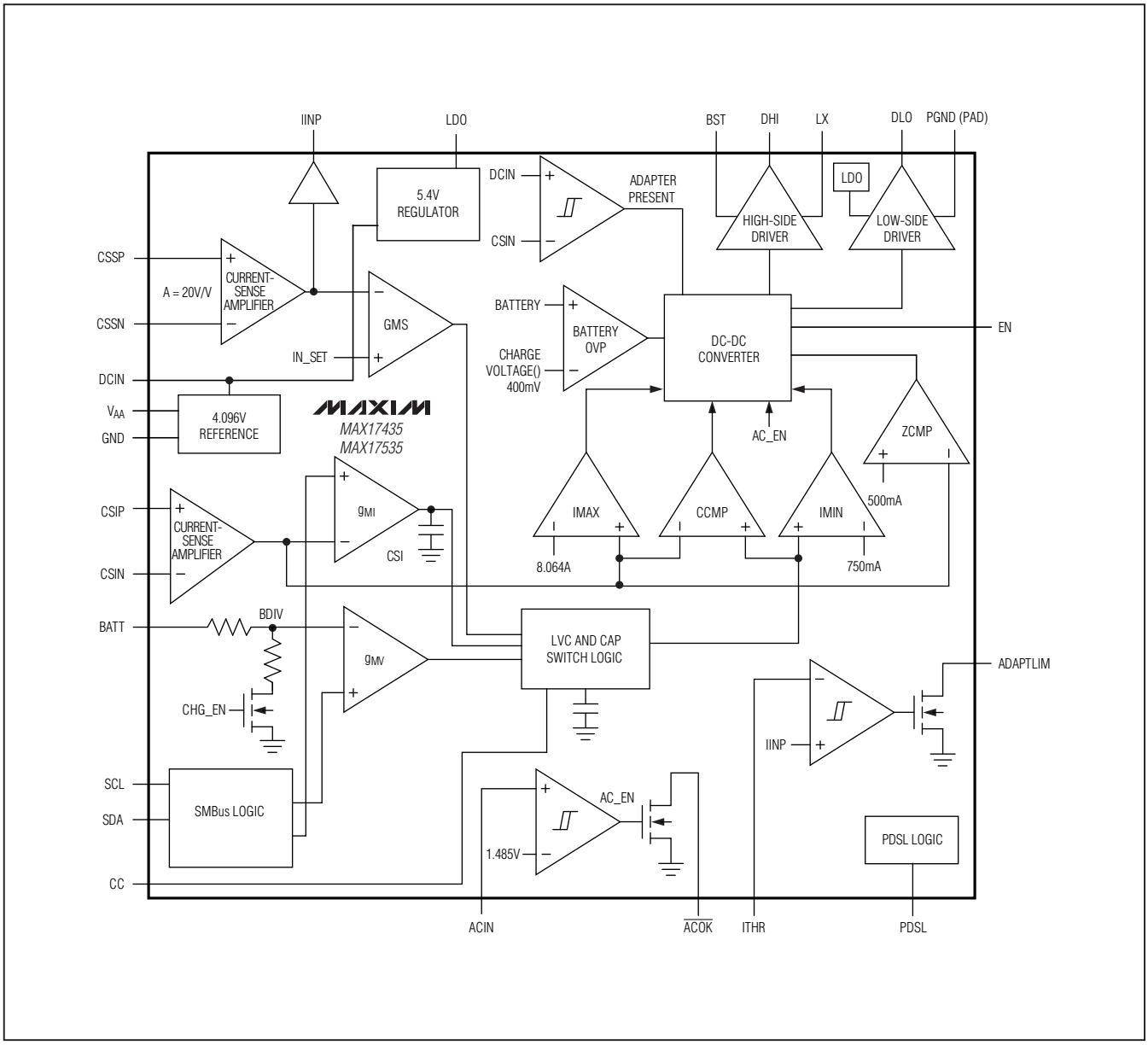

Figure 2. Block Diagram

The MAX17435/MAX17535 control input current (CCS control loop), charge current (CCI control loop), or charge voltage (CCV control loop), depending on the operating condition. The three control loops, CCV, CCI, and CCS, are brought together internally at the lowest voltage clamp (LVC) amplifier. The output of the LVC amplifier is the feedback control signal for the DC-DC controller. The minimum voltage at the CCV, CCI, or CCS appears at the output of the LVC amplifier and clamps the other control loops to within 0.3V above the control point. Clamping the other two control loops close to the lowest control loop ensures fast transition with minimal overshoot when switching between different control loops (see the *Compensation* section). The CCI loop is internally compensated and the CCV and CCS loops share a common compensation network at CC. The dominant control loop (CCV, CCS) drives the compensation network.

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Table 1. EN Pin Function

ADAPTER PRESENT	EN	PDSL STATUS	CHARGER STATUS	SYSTEM CURRENT MONITOR STATUS (IINP PATH)
Yes	High	PDSL is pumped 8V above the DCIN voltage (charge pump on).	Enabled	Enabled
Yes	Low	PDSL is pumped 8V above the DCIN voltage (charge pump on).	Disabled	Enabled
No	High	Charge pump is off and PDSL is forced to 0V (typ, 27C).	Disabled	Enabled
No	Low	Charge pump is off and PDSL is forced to 0V (typ, 27C).	Disabled	Disabled

EN Pin

The EN pin is a logic input. The state of the EN pin and the presence or absence of the adapter determines the state of PDSL, the IINP path, and the charger function as shown in Table 1.

30mA LDO

The 5.4V LDO is powered from DCIN and is compensated for loads from 0 to 30mA with a single 1µF ceramic capacitor. The load regulation over the 30mA load is 34mV (typ), 100mV max. The LDO supplies the drive for the DLO driver and also the BST circuitry. It is shut down when the adapter is absent.

Analog Input Current Monitor Output

IINP monitors the system-input current sensed across the sense resistor (RS1) that connects between CSSP and CSSN. The voltage at IINP is proportional to the input current according to the following equation:

$$I_{INPUT} = \frac{V_{IINP}}{RS1 \times A}$$

where I_{INPUT} is the DC current supplied by the AC adapter and A is the gain (20V/V typ). V_{IINP} has a 0V to 2.2V output voltage range.

Table 1 shows the charge and IINP status when the adapter is present or absent and as a function of the EN pin. When connected as shown in the standard application circuit, IINP monitors the input system current when the adapter is present or the battery discharge current when the adapter is absent. Leave IINP unconnected if not used.

Table 2 is the fault protection and shutdown operation table.

Table 2. Fault Protection and Shutdown Operation Table

MODE	CONTROLLER STATE	DRIVER STATE
Thermal fault (latched, reset by adapter reinsertion)	Charger disabled, PDSL low, LDO, and V_{AA} off	DHI and DLO low
ACOV fault or less than 3 ACOCP faults (not latched)	Charger disabled, PDSL low, LDO, and V_{AA} active	DHI and DLO low
More than 3 ACOCP faults (latched, reset by adapter reinsertion)	Charger disabled, PDSL low, LDO, and V_{AA} off	DHI and DLO low
Battery OV fault (not latched)	Charger disabled, PDSL high, LDO, and V_{AA} active	DHI and DLO low

SMBus Implementation

The MAX17435/MAX17535 receive control inputs from the SMBus interface. The MAX17435/MAX17535 use a subset of the commands documented in the System Management Bus Specifications V1.1, which can be downloaded from **www.smbus.org**. The MAX17435/MAX17535 use the SMBus read-word and write-word protocols to communicate with the system controller. The MAX17435/MAX17535 operate only as slave devices with address 0b0001001_ (0x12) and do not initiate communication on the bus. In addition, the MAX17435/MAX17535 have two identification registers: (0xFF), a 16-bit device ID register and a 16-bit manufacturer ID register (0xFE). The SMBus implementation is similar to the MAX8731A with the addition of the RELEARN() and IINPVoltage() commands. The SMBus is not powered from an external supply, so during states that disable the charger, the SMBus register data is lost, so the register data must be rewritten when reenabled. See Figure 3.

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pullup resistors for SDA and SCL to achieve rise times according to the SMBus specifications.

Communication starts when the master signals a START condition, which is a high-to-low transition on SDA, while SCL is high. When the master has finished communicating, the master issues a STOP condition, which is a low-to-high transition on SDA, while SCL is high. The bus is then free for another transmission. Figures 4 and 5 show the timing diagrams for signals on the SMBus interface.

The address byte, command byte, and data bytes are transmitted between the START and STOP conditions. The SDA state is allowed to change only while SCL is low, except for the START and STOP conditions. Data is transmitted in 8-bit bytes and is sampled on the rising edge of SCL. Nine clock cycles are required to transfer each byte in or out of the MAX17435/MAX17535 because either the master or the slave acknowledges the receipt of the correct byte during the ninth clock. The MAX17435/MAX17535 support the charger commands as described in Table 4.

a) Write-Word Format

S	SLAVE ADDRESS	W	ACK	COMMAND BYTE	ACK	LOW DATA BYTE	ACK	HIGH DATA BYTE	ACK	P
	7 bits	1b	1b	8 bits	1b	8 bits	1b	8 bits	1b	
	MSB LSB	0	0	MSB LSB	0	MSB LSB	0	MSB LSB	0	
	PRESET TO 0b0001001			Relearn() = 0x3D ChargingCurrent() = 0x14 ChargerVoltage() = 0x15		D7 D0		D15 D8		

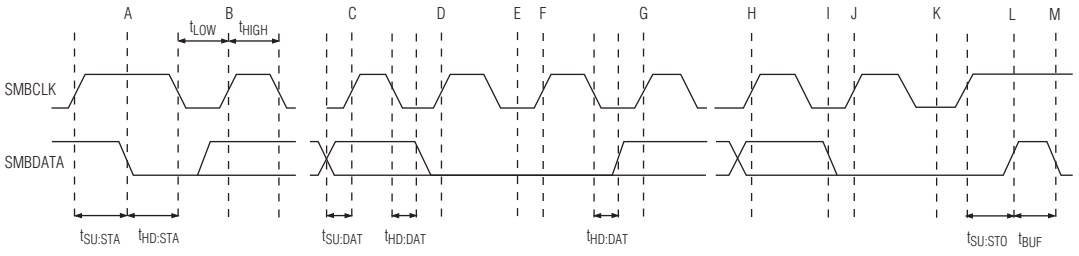
b) Read-Word Format

S	SLAVE ADDRESS	W	ACK	COMMAND BYTE	ACK	S	SLAVE ADDRESS	R	ACK	LOW DATA BYTE	ACK	HIGH DATA BYTE	NACK	P
	7 bits	1b	1b	8 bits	1b		7 bits	1b	1b	8 bits	1b	8 bits	1b	
	MSB LSB	0	0	MSB LSB	0		MSB LSB	1	0	MSB LSB	0	MSB LSB	1	
	PRESET TO 0b0001001			INP_Voltage() = 0x3E			PRESET TO 0b0001001			D7 D0		D15 D8		

LEGEND:
S = START CONDITION OR REPEATED START CONDITION
ACK = ACKNOWLEDGE (LOGIC-LOW)
W = WRITE BIT (LOGIC-LOW)
P = STOP CONDITION
NACK = NOT ACKNOWLEDGE (LOGIC-HIGH)
R = READ BIT (LOGIC-HIGH)

MASTER TO SLAVE
SLAVE TO MASTER

Figure 3. SMBus Write-Word and Read-Word Protocols



A = START CONDITION
B = MSB OF ADDRESS CLOCKED INTO SLAVE
C = LSB OF ADDRESS CLOCKED INTO SLAVE
D = R/$\overline{W}$ BIT CLOCKED INTO SLAVE
E = SLAVE PULLS SMBDATA LINE LOW
F = ACKNOWLEDGE BIT CLOCKED INTO MASTER
G = MSB OF DATA CLOCKED INTO SLAVE
H = LSB OF DATA CLOCKED INTO SLAVE
I = SLAVE PULLS SMBDATA LINE LOW
J = ACKNOWLEDGE CLOCKED INTO MASTER
K = ACKNOWLEDGE CLOCK PULSE
L = STOP CONDITION, DATA EXECUTED BY SLAVE
M = NEW START CONDITION

Figure 4. SMBus Write Timing

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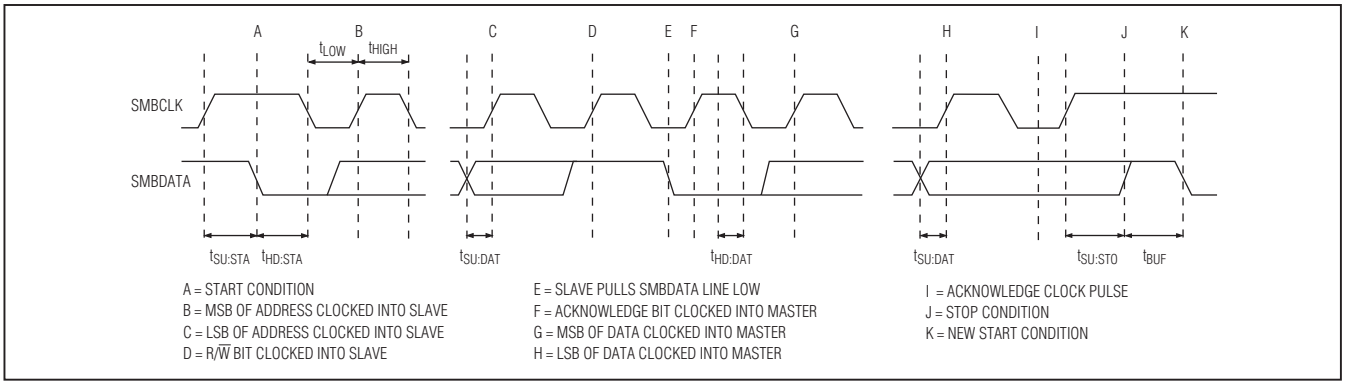

Figure 5. SMBus Read Timing

Battery Charger Commands

The MAX17435/MAX17535 support four battery-charger commands that use either write-word or read-word protocols as summarized in Table 3. ManufacturerID() and DeviceID() can be used to identify the MAX17435/MAX17535. On the MAX17435/MAX17535, ManufacturerID() always returns 0x004D and DeviceID() always returns 0x0008.

Setting Charge Voltage

To set the output voltage, use the SMBus to write a 16-bit ChargeVoltage() command using the data format listed in Table 4. The ChargeVoltage() command uses the write-word and read-word protocols (see Figure 3). The command code for ChargeVoltage() is 0x15 (0b00010101). The MAX17435/MAX17535 provide a charge-voltage range of 4.095V to 19.200V, with 16mV resolution. Set ChargeVoltage() below 4.095V to terminate charging. Upon reset, the ChargeVoltage() and ChargeCurrent() values are cleared and the charger remains off until both the ChargeVoltage() and the ChargeCurrent() command are sent. Both DHI and DLO remain low until the charger is restarted.

Setting Charge Current

To set the charge current, use the SMBus to write a 16-bit ChargeCurrent() command using the data format listed in Table 5. The ChargeCurrent() command uses the write-word and read-word protocols (see Figure 3). The command code for ChargeCurrent() is 0x14 (0b00010100). When RS2 = 10mΩ, the MAX17435/MAX17535 provide a charge-current range of 128mA to 8.064A, with 128mA resolution. If a sense resistor other than 10mΩ is used, the current limit must be scaled by RS/10mΩ, where RS is the sense resistor value used on the circuit. Set ChargeCurrent() to 0 to terminate charging. Upon reset, the ChargeVoltage() and ChargeCurrent() values are cleared and the charger remains off until both the ChargeVoltage() and the ChargeCurrent() command are sent. Both DHI and DLO remain low until the charger is restarted.

The MAX17435/MAX17535 include a fault limiter for low-battery conditions. If the battery voltage is less than 3V, the charge current is temporarily set to 128mA. The ChargeCurrent() register is preserved and becomes active again when the battery voltage is higher than 3V. This function effectively provides a foldback current limit that protects the charger during short circuit and overload.

Table 3. Battery Charger Command Summary

COMMAND	COMMAND NAME	READ/WRITE	DESCRIPTION	POR STATE
0x14	ChargeCurrent()	Read and write	6-bit charge-current setting, readback (3'b0, 6'bx, 7'b0)	0x0000
0x15	ChargeVoltage()	Read and write	11-bit charge-voltage setting, readback (1'b0, 11'bx, 4'b0)	0x0000
0x3D	Relearn Voltage	Read and write	11-bit relearn voltage set and 1-bit enable/status	0x4B00
0x3E	IINPVoltage()	Read only	Digital readback of IINP voltage	NA
0x3F	InputCurrent()	Read and write	6-bit input-current setting readback (3'b0, 6'bx, 7'b0)	0x1000
0xFE	ManufacturerID()	Read only	Manufacturer ID	0x004D
0xFF	DeviceID()	Read only	Device ID	0x0008

Note: *'x' means the data is sent to the analog block.*

Table 4. ChargeVoltage() (0x15)

BIT	BIT NAME	DESCRIPTION
0	—	Not used. Normally a 1mV weight.
1	—	Not used. Normally a 2mV weight.
2	—	Not used. Normally a 4mV weight.
3	—	Not used. Normally an 8mV weight.
4	Charge Voltage, DACV 0	0 = Adds 0mV of charger voltage compliance, 4095mV min. 1 = Adds 16mV of charger voltage compliance.
5	Charge Voltage, DACV 1	0 = Adds 0mV of charger voltage compliance, 4095mV min. 1 = Adds 32mV of charger voltage compliance.
6	Charge Voltage, DACV 2	0 = Adds 0mV of charger voltage compliance, 4095mV min. 1 = Adds 64mV of charger voltage compliance.
7	Charge Voltage, DACV 3	0 = Adds 0mV of charger voltage compliance, 4095mV min. 1 = Adds 128mV of charger voltage compliance.
8	Charge Voltage, DACV 4	0 = Adds 0mV of charger voltage compliance, 4095mV min. 1 = Adds 256mV of charger voltage compliance.
9	Charge Voltage, DACV 5	0 = Adds 0mV of charger voltage compliance, 4095mV min. 1 = Adds 512mV of charger voltage compliance.
10	Charge Voltage, DACV 6	0 = Adds 0mA of charger voltage compliance, 4095mV min. 1 = Adds 1024mV of charger voltage compliance.
11	Charge Voltage, DACV 7	0 = Adds 0mV of charger voltage compliance, 4095mV min. 1 = Adds 2048mV of charger voltage compliance.
12	Charge Voltage, DACV 8	0 = Adds 0mV of charger voltage compliance. 1 = Adds 4096mV of charger voltage compliance.
13	Charge Voltage, DACV 9	0 = Adds 0mV of charger voltage compliance. 1 = Adds 8192mV of charger voltage compliance.
14	Charge Voltage, DACV 10	0 = Adds 0mV of charger voltage compliance. 1 = Adds 16384mV of charger voltage compliance, 19200mV max.
15	—	Not used. Normally a 32768mV weight.

Table 5. ChargeCurrent() (0x14) (10mΩ Sense Resistor, RS2)

BIT	BIT NAME	DESCRIPTION
0	—	Not used. Normally a 1mA weight.
1	—	Not used. Normally a 2mA weight.
2	—	Not used. Normally a 4mA weight.
3	—	Not used. Normally an 8mA weight.
4	—	Not used. Normally a 16mA weight.
5	—	Not used. Normally a 32mA weight.
6	—	Not used. Normally a 64mA weight.
7	Charge Current, DACI 0	0 = Adds 0mA of charger current compliance. 1 = Adds 128mA of charger current compliance.
8	Charge Current, DACI 1	0 = Adds 0mA of charger current compliance. 1 = Adds 256mA of charger current compliance.

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Table 5. ChargeCurrent() (0x14) (10mΩ Sense Resistor, RS2) (continued)

BIT	BIT NAME	DESCRIPTION
9	Charge Current, DACI 2	0 = Adds 0mA of charger current compliance. 1 = Adds 512mA of charger current compliance.
10	Charge Current, DACI 3	0 = Adds 0mA of charger current compliance. 1 = Adds 1024mA of charger current compliance.
11	Charge Current, DACI 4	0 = Adds 0mA of charger current compliance. 1 = Adds 2048mA of charger current compliance.
12	Charge Current, DACI 5	0 = Adds 0mA of charger current compliance. 1 = Adds 4096mA of charger current compliance, 8064mA max
13	—	Not used. Normally a 8192mA weight.
14	—	Not used. Normally a 16386mA weight.
15	—	Not used. Normally a 32772mA weight.

Setting Input-Current Limit

System current normally fluctuates as portions of the system are powered up or put to sleep. By using the input-current-limit circuit, the output-current requirement of the AC wall adapter can be lowered, reducing system cost.

The total input current is the sum of the system supply current, the charge current flowing into the battery, and the current required by the charger. When the input current exceeds the input current limit set with the InputCurrent() command, the MAX17435/MAX17535 reduce the charge current to provide priority to system load current. As the system supply current increases, the charge current is reduced as needed to maintain the total input current at the input current limit. The MAX17435/MAX17535 decrease the charge current to zero, if necessary, to reduce the input current to the input current limit. Thereafter, if the system current continues to increase, there is nothing the MAX17435/MAX17535 can do to maintain the input current at the input current limit. If the system current continues to increase so that the input current exceeds the ACOCP threshold (130% of InputCurrent() setting) for more than 16ms (typ), the MAX17435/MAX17535 drive PDSL low, which turns off the adapter selector FETs and disconnects the adapter from the system. After waiting 0.6s, the MAX17435/MAX17535 re-enable PDSL. If the ACOCP fault occurs again, the MAX17435/MAX17535 drive PDSL low again after the 16ms (typ) delay. This cycle is repeated a maximum of three times, after which the MAX17435/MAX17535 are latched off, and need to be reset by removing and reinserting the adapter.

The total input current can be estimated as follows:

$$I_{INPUT} = I_{SYSTEM} + I_{CHARGER} + [(I_{CHARGE} \times V_{BATTERY})/(V_{IN} \times \eta)]$$

where η is the efficiency of the DC-DC converter (typically 85% to 95%).

To set the input current limit, use the SMBus to write a 16-bit InputCurrent() using the data format listed in Table 6. The InputCurrent() command uses the write-word and read-word protocols (see Figure 3). The command code for InputCurrent() is 0x3F (0b00111111). When RS1 = 10mΩ, the MAX17435/MAX17535 provide an input current-limit range of 256mA to 11.004A with 256mA resolution. If a resistor RS other than 10mΩ is used, the input current limit is scaled by a factor of 10mΩ/RS1. InputCurrent() settings from 1mA to 256mA result in a current limit of 256mA. Upon reset, the input current limit is 256mA.

Setting Relearn Voltage

To set the relearn voltage, use the SMBus to write a 16-bit RelearnVoltage() command using the data format listed in Table 7. The RelearnVoltage() command uses the write-word and read-word protocols (see Figure 3). The command code for RelearnVoltage() is 0x3D (0b00111101). The MAX17435/MAX17535 provide a charge-voltage range of 4.095V to 19.200V with 16mV resolution. When the relearn function is enabled by setting bit 0 to 1, the MAX17435/MAX17535 drive PDSL low, turning off the adapter selector FETs and turning on the battery selector FET. This allows the battery to discharge by powering the system while the adapter is still present. The battery voltage is monitored until the battery voltage reaches the relearn voltage corresponding to a known low state of charge. The relearn bit 0 is set to zero, and PDSL is re-enabled.

Table 6. InputCurrent() (0x3F) (10mΩ Sense Resistor, RS1)

BIT	BIT NAME	DESCRIPTION
0	—	Not used. Normally a 2mA weight.
1	—	Not used. Normally a 4mA weight.
2	—	Not used. Normally an 8mA weight.
3	—	Not used. Normally a 16mA weight.
4	—	Not used. Normally a 32mA weight.
5	—	Not used. Normally a 64mA weight.
6	—	Not used. Normally a 128mA weight.
7	Input Current, DACS 0	0 = Adds 0mA of input current compliance. 1 = Adds 256mA of input current compliance.
8	Input Current, DACS 1	0 = Adds 0mA of input current compliance. 1 = Adds 512mA of input current compliance.
9	Input Current, DACS 2	0 = Adds 0mA of input current compliance. 1 = Adds 1024mA of input current compliance.
10	Input Current, DACS 3	0 = Adds 0mA of input current compliance. 1 = Adds 2048mA of input current compliance.
11	Input Current, DACS 4	0 = Adds 0mA of input current compliance. 1 = Adds 4096mA of input current compliance.
12	Input Current, DACS 5	0 = Adds 0mA of input current compliance. 1 = Adds 8192mA of input current compliance, 11004mA max.
13	—	Not used. Normally a 16384mA weight.
14	—	Not used. Normally a 32768mA weight.
15	—	Not used. Normally a 65536mA weight.

Table 7. Relearn() (0x3D)

BIT	BIT NAME	DESCRIPTION
0	Relearn, RL 0	0 = Disables the relearn function. 1 = Enables the relearn function. When the relearn threshold is crossed as the battery discharges, bit 0 is reset to zero by the MAX17435/MAX17535.
1	—	Not used.
2	—	Not used.
3	—	Not used.
4	Relearn, RL 1	0 = Adds 0mV of relearn threshold compliance, 1024mV min. 1 = Adds 16mV of relearn threshold compliance.
5	Relearn, RL 2	0 = Adds 0mV of relearn threshold compliance, 1024mV min. 1 = Adds 32mV of relearn threshold compliance.
6	Relearn, RL 3	0 = Adds 0mV of relearn threshold compliance, 1024mV min. 1 = Adds 64mV of relearn threshold compliance.
7	Relearn, RL 4	0 = Adds 0mV of relearn threshold compliance, 1024mV min. 1 = Adds 128mV of relearn threshold compliance.
8	Relearn, RL 5	0 = Adds 0mV of relearn threshold compliance, 1024mV min. 1 = Adds 256mV of relearn threshold compliance.

Table 7. Relearn() (0x3D) (continued)

BIT	BIT NAME	DESCRIPTION
9	Relearn, RL 6	0 = Adds 0mV of relearn threshold compliance, 1024mV min. 1 = Adds 512mV of relearn threshold compliance.
10	Relearn, RL 7	0 = Adds 0mA of relearn threshold compliance. 1 = Adds 1024mV of relearn threshold compliance.
11	Relearn, RL 8	0 = Adds 0mV of relearn threshold compliance. 1 = Adds 2048mV of relearn threshold compliance.
12	Relearn, RL 9	0 = Adds 0mV of relearn threshold compliance. 1 = Adds 4096mV of relearn threshold compliance.
13	Relearn, RL 10	0 = Adds 0mV of relearn threshold compliance. 1 = Adds 8192mV of relearn threshold compliance.
14	Relearn, RL 11	0 = Adds 0mV of relearn threshold compliance. 1 = Adds 16384mV of relearn threshold compliance, 19200mV max.
15	—	Not used.

Reading IINP Voltage

To read the digital version of the IINP voltage, issue the SMBus command IINPVoltage() command using the 16-bit data format listed in Table 8. The command code for IINPVoltage() is 0x3E (0b00111110). The IINPVoltage() command uses the read-word protocol (see Figure 3).

Charger Timeout

The MAX17435/MAX17535 include a timer to terminate charging if the charger has not received a ChargeVoltage() or ChargeCurrent() command within 140s (min). If a timeout occurs, both ChargeVoltage() and ChargeCurrent() commands must be sent again to reenable charging.

Table 8. IINPVoltage() (0x3E)

BIT	BIT NAME	DESCRIPTION
0	—	Not used. Normally a 1mV weight.
1	—	Not used. Normally a 2mV weight.
2	—	Not used. Normally a 4mV weight.
3	—	Not used. Normally a 8mV weight.
4	IINP Voltage, DACV 0	0 = Adds 0mV of IINP voltage. 1 = Adds 12.8mV of IINP voltage.
5	IINP Voltage, DACV 1	0 = Adds 0mV of IINP voltage. 1 = Adds 25.6mV of IINP voltage.
6	IINP Voltage, DACV 2	0 = Adds 0mV of IINP voltage. 1 = Adds 51.2mV of IINP voltage.
7	IINP Voltage, DACV 3	0 = Adds 0mV of IINP voltage. 1 = Adds 103.6mV of IINP voltage.
8	IINP Voltage, DACV 4	0 = Adds 0mV of IINP voltage. 1 = Adds 207.2mV of IINP voltage.
9	IINP Voltage, DACV 5	0 = Adds 0mV of IINP voltage. 1 = Adds 414.4mV of IINP voltage.

Table 8. IINPVoltage() (0x3E) (continued)

BIT	BIT NAME	DESCRIPTION
10	IINP Voltage, DACV 6	0 = Adds 0mA of IINP voltage. 1 = Adds 828.8mV of IINP voltage.
11	IINP Voltage, DACV 7	0 = Adds 0mV of IINP voltage. 1 = Adds 1.6576V of IINP voltage to a maximum of 2.20V.
12	—	Not used. Normally a 4096mV weight.
13	—	Not used. Normally a 8192mV weight.
14	—	Not used. Normally a 16384mV weight.
15	—	Not used. Normally a 32768mV weight.

DC-DC Converter

The MAX17435/MAX17535 employ a synchronous step-down DC-DC converter with an n-channel, high-side MOSFET switch and an n-channel low-side synchronous rectifier. The MAX17435/MAX17535 feature a pseudo-fixed-frequency, current-mode control scheme with cycle-by-cycle current limit. The controller's constant off-time (t_{OFF}) is calculated based on V_{DCIN}, V_{CSIN}, and a time constant with a minimum value of 300ns. The MAX17435/MAX17535 can also operate in discontinuous conduction mode for improved light-load efficiency. The operation of the DC-DC controller is determined by the following five comparators as shown in the block diagram in Figure 2:

- The **IMIN** comparator sets the peak inductor current in discontinuous mode. IMIN compares the control signal (LVC) against 100mV (typ). When LVC voltage is less than 100mV, DHI and DLO are both low.
- The **CCMP** comparator is used for current-mode regulation in continuous conduction mode. CCMP compares LVC against the charging current feedback signal (CSI). The comparator output is high and the high-side MOSFET on-time is terminated when the CSI voltage is higher than LVC.
- The **IMAX** comparator provides a cycle-by-cycle current limit. IMAX compares CSI to 2V (corresponding to 10A when RS2 = 10mΩ). The comparator output is high and the high-side MOSFET on-time is terminated when the current-sense signal exceeds 10A. A new cycle cannot start until the IMAX comparator output goes low.
- The **ZCMP** comparator provides zero-crossing detection during discontinuous conduction. ZCMP compares the current-sense feedback signal to 500mA (RS2 = 10mΩ). When the inductor current is lower than the 500mA threshold, the comparator output is high and DLO is turned off.
- The **OVP** comparator checks for the battery voltage 400mV above the set point and, if that condition is detected, it disables charging.

CCV, CCI, CCS, and LVC Control Blocks

The MAX17435/MAX17535 control input current (CCS control loop), charge current (CCI control loop), or charge voltage (CCV control loop), depending on the operating condition. The three control loops, CCV, CCI, and CCS are brought together internally at the lowest voltage clamp (LVC) amplifier. The output of the LVC amplifier is the feedback control signal for the DC-DC controller. The minimum voltage at the CCV, CCI, or CCS appears at the output of the LVC amplifier and clamps the other control loops to within 0.3V above the control point. Clamping the other two control loops close to the lowest control loop ensures fast transition with minimal overshoot when switching between different control loops (see the *Compensation* section).

Continuous Conduction Mode

With sufficient charge current, the MAX17435/MAX17535s' inductor current never crosses zero, which is defined as continuous conduction mode. The MAX17435 switches at 850kHz (nominal) and the MAX17535 switches at 500kHz (nominal) if the charger is not in dropout (V_{CSIN} < 0.88 x V_{DCIN}). The controller starts a new cycle by turning on the high-side MOSFET and turning off the low-side MOSFET. When the charge current feedback signal (CSI) is greater than the control point (LVC), the CCMP comparator output goes high and the controller initiates the off-time by turning off the high-side MOSFET and turning on the low-side MOSFET. The operating frequency is governed by the off-time and is dependent upon V_{CSIN} and V_{DCIN}.

At the end of the fixed off-time, the controller initiates a new cycle if the control point (LVC) is greater than 150mV, and the peak charge current is less than the cycle-by-cycle current limit. Restated another way, IMIN must be high, IMAX must be low, and OVP must be low for the

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controller to initiate a new cycle. If the peak inductor current exceeds IMAX comparator threshold or the output voltage exceeds the OVP threshold, then the on-time is terminated. The cycle-by-cycle current limit effectively protects against overcurrent and short-circuit faults.

If, during the off-time, the inductor current goes to zero, the ZCMP comparator output pulls high, turning off the low-side MOSFET. Both the high- and low-side MOSFETs are turned off until another cycle is ready to begin. The MAX17435/MAX17535 enter into the discontinuous conduction mode (see the *Discontinuous Conduction* section).

The on-time is calculated according to the following equation:

$$t_{ON} = \frac{L \times I_{RIPPLE}}{V_{CSSN} - V_{BATT}}$$

where:

$$I_{RIPPLE} = \frac{V_{BATT} \times t_{OFF}}{L}$$

There is a 0.3µs minimum off-time when the (V_{DCIN} - V_{BATT}) differential becomes too small. If $V_{BATT} \geq 0.88 \times V_{DCIN}$, then the threshold for minimum off-time is reached and the off-time is fixed at 0.27µs. The switching frequency in this mode varies according to the equation:

$$f = \frac{1}{\frac{L \times I_{RIPPLE}}{V_{CSSN} - V_{BATT}} + t_{OFF}}$$

Discontinuous Conduction

The MAX17435/MAX17535 can also operate in discontinuous conduction mode to ensure that the inductor current is always positive. The MAX17435/MAX17535 enter discontinuous conduction mode when the output of the LVC control point falls below 110mV. For RS2 = 10mΩ, this corresponds to 367mA:

$$I_{DIS} = \frac{1}{2} \times \frac{110mV}{15 \times RS2} = 367mA$$

where I_{DIS} is the current level for discontinuous conduction.

In discontinuous mode, a new cycle is not started until the LVC voltage rises above 150mV. Discontinuous mode operation can occur during conditioning charge of overdischarged battery packs, when the charge current has been reduced sufficiently by the CCS control loop, or when the charger is in constant-voltage mode with a nearly full battery pack.

Under extremely light loads, the BST capacitor may become discharged if there is no DLO pulse. After 192µs (typ), the MAX17435/MAX17535 turn on DLO for 300ns and 550ns, respectively, to recharge the BST capacitor. This DLO pulse need not be followed by a DHI pulse.

Compensation

The CCI loop is internally compensated. The CCV and the CCS share the external compensation capacitor. The control loop, which is dominant, uses the external compensation cap and the one that is not used uses an internal compensation capacitor.

CCV Loop Compensation

The simplified schematic in Figure 6 is sufficient to describe the operation of the MAX17435/MAX17535 when the voltage loop (CCV) is in control. The required compensation network is a pole-zero pair formed with C_{CC} and R_{CC}, which is an internal 1.7kΩ. The pole is necessary to roll off the voltage loop's response at low frequency; C_{CC} = 330pF is sufficient for most applications.

MOSFET Drivers

The DHI and DLO outputs are optimized for driving moderate-sized power MOSFETs. The MOSFET drive capability is the same for both the low-side and high-sides switches. This is consistent with the variable duty factor that occurs in the notebook computer environment where the battery voltage changes over a wide range. There must be a low-resistance, low-inductance path from the DLO driver to the MOSFET gate to prevent shoot-through. Otherwise, the sense circuitry in the MAX17435/MAX17535 interprets the MOSFET gate as off while there is still charge left on the gate. Use very short, wide traces measuring 10 squares to 20 squares or less (1.25mm to 2.5mm wide if the MOSFET is 25mm from the device). Unlike the DLO output, the DHI output uses a 50ns (typ) delay time to prevent the low-side MOSFET from turning on until DHI is fully off. The same considerations should be used for routing the DHI signal to the high-side MOSFET.

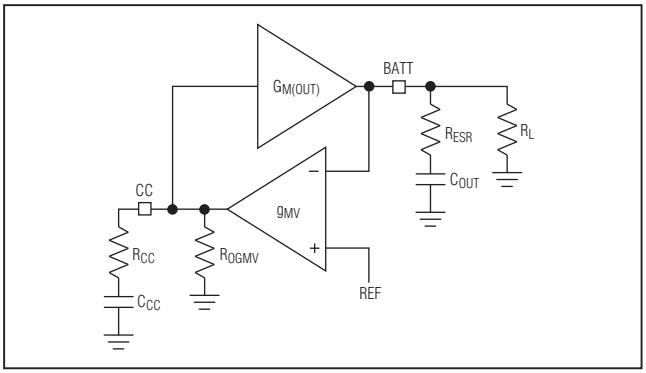

Figure 6. CC Loop Diagram

The high-side driver (DHI) swings from LX to 5V above LX (BST) and has a typical impedance of 1.5Ω sourcing and 0.8Ω sinking. The low-side driver (DLO) swings from DLOV to ground and has a typical impedance of 3Ω sinking and 3Ω sourcing. This helps prevent DLO from being pulled up when the high-side switch turns on due to capacitive coupling from the drain to the gate of the low-side MOSFET. This places some restrictions on the MOSFETs that can be used. Using a low-side MOSFET with smaller gate-to-drain capacitance can prevent these problems.

Design Procedure

MOSFET Selection

Choose the n-channel MOSFETs according to the maximum required charge current. Low-current applications usually require less attention. The high-side MOSFET (N1) must be able to dissipate the resistive losses plus the switching losses at both $V_{DCI(MIN)}$ and $V_{DCIN(MAX)}$. Calculate both these sums.

Ideally, the losses at $V_{DCIN(MIN)}$ should be roughly equal to losses at $V_{DCIN(MAX)}$ with lower losses in between. If the losses at $V_{DCIN(MIN)}$ are significantly higher than the losses at $V_{DCIN(MAX)}$, consider increasing the size of N1. Conversely, if the losses at $V_{DCIN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider reducing the size of N1. If DCIN does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses. Choose a low-side MOSFET that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., one or two 8-pin SO, DPAK, or D^2 PAK), and is reasonably priced. Make sure that the DLO gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems can occur. Select devices that have short turn-off times, and make sure that:

$$N2(t_{DOFF(MAX)}) - N1(t_{DON(MIN)}) < 40ns, \text{ and}$$
$$N1(t_{DOFF(MAX)}) - N2(t_{DON(MIN)}) < 40ns$$

Failure to do so could result in efficiency-reducing shoot-through currents.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET, the worst-case power dissipation (PD) due to resistance occurs at the minimum supply voltage:

$$PD(High\text{-}side) = \left(\frac{V_{BATT}}{V_{DCIN}}\right)\left(\frac{I_{LOAD}}{2}\right)^2 \times R_{DS(ON)}$$

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often limits how small the MOSFET can be. The optimum occurs when the switching (AC) losses equal the conduction ($R_{DS(ON)}$) losses. Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied, due to the squared term in the $CV^2 f$ switching-loss equation. If the high-side MOSFET that was chosen for adequate $R_{DS(ON)}$ at low supply voltages becomes extraordinarily hot when subjected to $V_{IN(MAX)}$, then choose a MOSFET with lower losses. Calculating the power dissipation in N1 due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including a verification using a thermocouple mounted on N1:

$$PD(HS\_Switching) = \frac{V_{DCIN(MAX)}^2 \times C_{RSS} \times f_{SW} \times I_{LOAD}}{2 \times I_{GATE}}$$

where C_{RSS} is the reverse transfer capacitance of N1 and I_{GATE} is the peak gate-drive source/sink current (3.3A sourcing and 5A sinking).

For the low-side MOSFET (N2), the worst-case power dissipation always occurs at maximum input voltage:

$$PD(Low\text{-}side) = \left[1 - \left(\frac{V_{BATT}}{V_{DCIN}}\right)\right]\left(\frac{I_{LOAD}}{2}\right)^2 \times R_{DS(ON)}$$

Inductor Selection

The charge current, ripple, and operating frequency (off-time) determine the inductor characteristics. For optimum efficiency, choose the inductance according to the following equation:

$$L = V_{BATT} \times t_{OFF}/(0.3 \times I_{CHG})$$

This sets the ripple current to 1/3 the charge current and results in a good balance between inductor size and efficiency. Higher inductor values decrease the ripple current. Smaller inductor values require high saturation current capabilities and degrade efficiency.

Due to the minimum t_{OFF} blanking effect upon zero-crossing detection, higher inductor values are desired for proper operation for a design with low input voltage and high output voltage, especially for MAX17535.

Inductor L1 must have a saturation current rating of at least the maximum charge current plus 1/2 the ripple current (ΔI_L):

$$I_{SAT} = I_{CHG} + (1/2)\,\Delta I_L$$

The ripple current is determined by:

$$\Delta I_L = V_{BATT} \times t_{OFF}/L$$

where:

$$t_{OFF} = 2.5\mu s\,(V_{DCIN} - V_{BATT})/V_{DCIN} \text{ for } V_{BATT} < 0.88\,V_{DCIN}$$

or:

$$t_{OFF} = 0.3\mu s \text{ for } V_{BATT} > 0.88\,V_{DCIN}$$

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. Nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resilience to power-up surge currents:

$$I_{RMS} = I_{CHG}\left(\frac{\sqrt{V_{BATT}(V_{DCIN} - V_{BATT})}}{V_{DCIN}}\right)$$

The input capacitors should be sized so that the temperature rise due to ripple current in continuous conduction does not exceed approximately 10°C. The maximum ripple current occurs at 50% duty factor or $V_{DCIN} = 2 \times V_{BATT}$, which equates to $0.5 \times I_{CHG}$. If the application of interest does not achieve the maximum value, size the input capacitors according to the worst-case conditions.

Output Capacitor Selection

The output capacitor absorbs the inductor ripple current and must tolerate the surge current delivered from the battery when it is initially plugged into the charger. As such, both capacitance and ESR are important parameters in specifying the output capacitor as a filter and to the ensure stability of the DC-DC converter. See the *Compensation* section. Beyond the stability requirements, it is often sufficient to make sure that the output capacitor's ESR is much lower than the battery's ESR. Either tantalum or ceramic capacitors can be used on the output. Ceramic devices are preferable because of their good voltage ratings and resilience to surge currents. For most applications the output capacitance can be as low as 4.7µF. If the output voltage is low and the input voltage is high, the output capacitance may need to be increased.

Applications Information

Layout and Bypassing

Bypass DCIN with a 0.1µF ceramic to ground (Figure 1). N3 and Q1A protect the MAX17435/MAX17535 when the DC power source input is reversed. Bypass V_{CC}, DCIN, LDO, and V_{AA}, as shown in Figure 1.

Good PCB layout is required to achieve specified noise immunity, efficiency, and stable performance. The PCB layout artist must be given explicit instructions—preferably, a sketch showing the placement of the power switching components and high current routing. Refer to the PCB layout in the MAX17435 and MAX17535 Evaluation Kits for examples. A ground plane is essential for optimum performance. In most applications, the circuit is located on a multilayer board, and full use of the four or more copper layers is recommended. Use the top layer for high current connections, the bottom layer for quiet connections, and the inner layers for an uninterrupted ground plane.

Use the following step-by-step guide:

1) Place the high-power connections first, with their grounds adjacent:
   - Minimize the current-sense resistor trace lengths, and ensure accurate current sensing with Kelvin connections.
   - Minimize ground trace lengths in the high-current paths.
   - Minimize other trace lengths in the high-current paths.
   - Use > 5mm wide traces in the high-current paths.
   - Connect C1 and C2 to high-side MOSFET (10mm max length).
   - Minimize the LX node (MOSFETs, rectifier cathode, inductor (15mm max length). Keep LX on one side of the PCB to reduce EMI radiation.

Ideally, surface-mount power components are flush against one another with their ground terminals almost touching. These high-current grounds are then connected to each other with a wide, filled zone of top-layer copper, so they do not go through vias. The resulting top-layer subground plane is connected to the normal inner-layer ground plane at the paddle. Other high-current paths should also be minimized, but focusing primarily on short ground and current-sense connections eliminates about 90% of all PCB layout problems.

2) Place the IC and signal components. Keep the main switching node (LX node) away from sensitive analog components (current-sense traces and V_{AA} capacitor). **Important:** The IC must be no further than 10mm from the current-sense resistors. Quiet connections to V_{AA}, CC, ACIN, and DCIN should be returned to a separate ground (GND) island. The appropriate traces are marked on the schematic with the () ground symbol. There is very little current flowing in these traces, so the ground island need not be very large. When placed on an inner layer, a sizable ground island can help simplify the layout because the low current connections can be made through vias. The ground pad on the backside of the package should also be connected to this quiet ground island.
3) Keep the gate drive traces (DHI and DLO) as short as possible (L < 20mm), and route them away from the current-sense lines and REF. These traces should also be relatively wide (W > 1.25mm).
4) Place ceramic bypass capacitors close to the IC. The bulk capacitors can be placed further away. Place the current-sense input filter capacitors under the part, connected directly to the GND pin.
5) Use a single-point star ground placed directly below the part at the PGND pin. Connect the power ground (ground plane) and the quiet ground island at this location.

Refer to the MAX17435 and MAX17535 Evaluation Kit layouts for a layout example.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP	T2444+3	21-0139	90-0021

High-Frequency, Low-Cost SMBus Chargers

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/09	Initial release	—
1	9/10	Removed the MAX17035 from the data sheet	1–28