# R2J20601NP

## Driver – MOS FET Integrated SiP (DrMOS)

REJ03G0237-0500
Rev.5.00
Apr 10, 2006

## Description

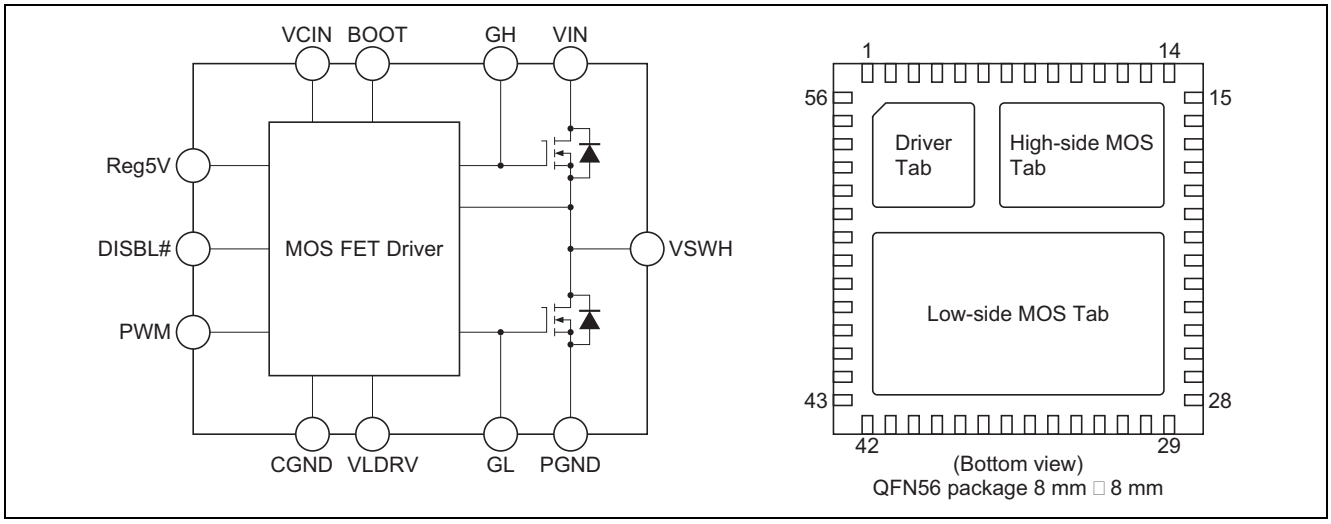
The R2J20601NP multi-chip module incorporates a high-side MOS FET, low-side MOS FET, and MOS-FET driver in a single QFN package. The on and off timing of the power MOS FET is optimized by the built-in driver, making this device suitable for large-current buck converters. The chip also incorporates a high-side bootstrap Schottky barrier diode (SBD), eliminating the need for an external SBD for this purpose.

Integrating a driver and both high-side and low-side power MOS FETs, the new device is also compliant with the package standard "Driver – MOS FET integrated SiP (DrMOS)" proposed by Intel Corporation.

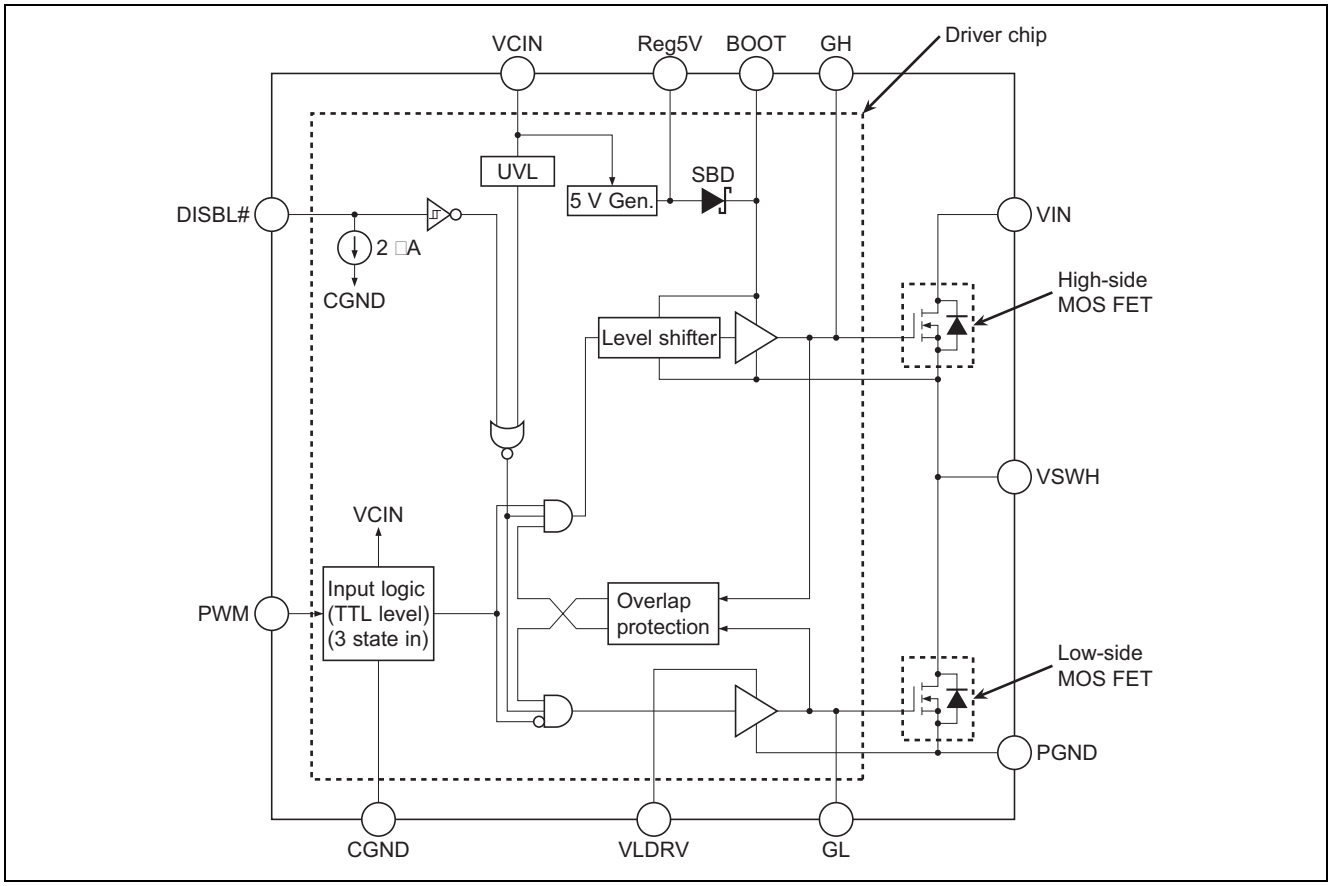
## Features

- Built-in power MOS FET suitable for applications with 12 V input and low output voltage
- Built-in driver circuit which matches the power MOS FET
- Built-in tri-state input function which can support a number of PWM controllers
- VIN operating-voltage range: 16 V max
- High-frequency operation (above 1 MHz) possible
- Large average output current (35 A)
- Achieve low power dissipation (About 5.6 W at 1 MHz, 25 A)
- Controllable driver: Remote on/off
- Built-in Schottky diode for bootstrapping
- Low-side drive voltage can be independently set
- Small package: QFN56 (8 mm × 8 mm × 0.8 mm)

## Outline



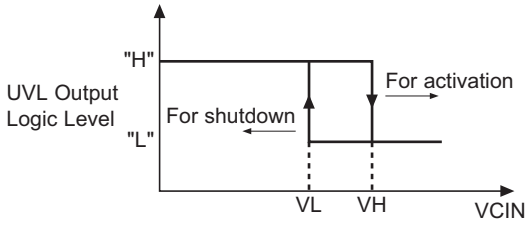
## Block Diagram



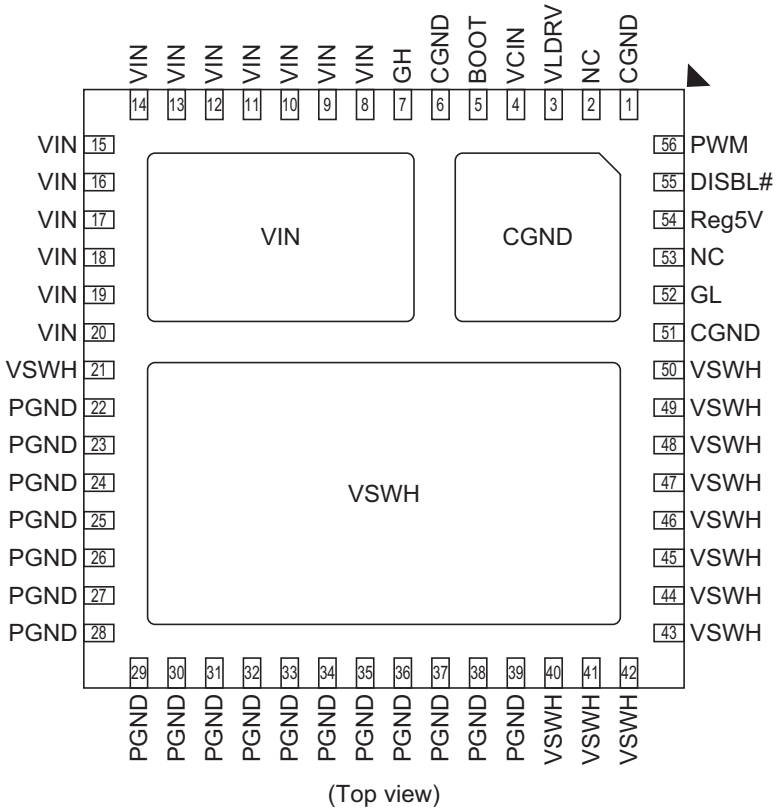

Notes: 1. Truth table for the DISBL# pin.

| DISBL# Input | Driver Chip Status |
|---|---|
| “L” | Shutdown (GL, GH = “L”) |
| “Open” | Shutdown (GL, GH = “L”) |
| “H” | Enable (GL, GH = “Active”) |

2. Output signal from the UVL block



## Pin Arrangement




(Top view)

## Pin Description

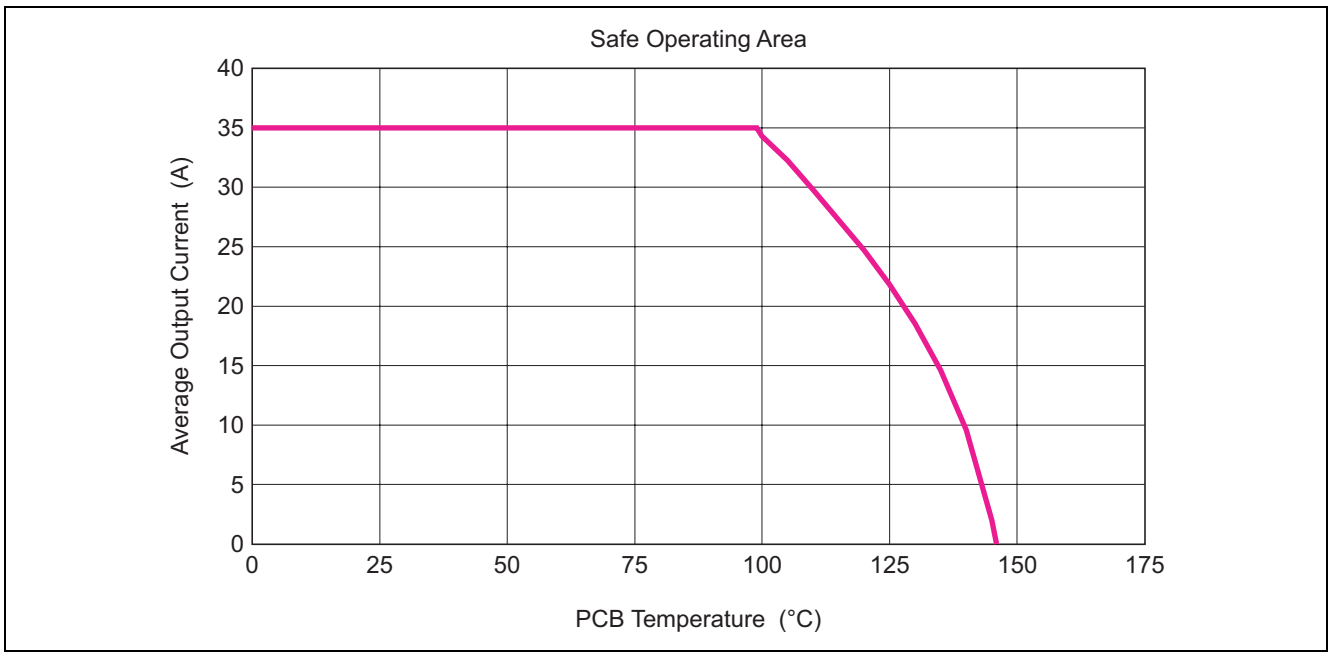
| Pin Name | Pin No. | Description | Remarks |
|---|---|---|---|
| CGND | 1, 6, 51, Tab | Control signal ground | Should be connected to PGND externally |
| NC | 2, 53 | No connect | |
| VLDRV | 3 | Low side gate supply voltage | For 5 V to 12 V gate drive voltage for Low side gate driver |
| VCIN | 4 | Control input voltage (+12 V input) | Driver Vcc input |
| BOOT | 5 | Bootstrap voltage pin | To be supplied +5 V through internal SBD |
| GH | 7 | High side gate signal | Pin for Monitor |
| VIN | 8 to 20, Tab | Input voltage | |
| VSWH | 21, 40 to 50, Tab | Phase output/Switch output | |
| PGND | 22 to 39 | Power ground | |
| GL | 52 | Low side gate signal | Pin for Monitor |
| Reg5V | 54 | +5 V logic power supply output | |
| DISBL# | 55 | Signal disable | Disabled when DISBL# is “L” |
| PWM | 56 | PWM drive logic input | |

## Absolute Maximum Ratings

(Ta = 25°C)

| Item | Symbol | Rating | Units | Note |
|---|---|---|---|---|
| Power dissipation | Pt(25) | 25 | W | 1 |
| | Pt(110) | 8 | W | 1 |
| Average output current | Iout | 35 | A | |
| Input voltage | VIN (DC) | –0.3 to +16 | V | 2 |
| | VIN (AC) | 20 | | 2, 6 |
| Supply voltage | VCIN (DC) | –0.3 to +16 | V | 2 |
| | VCIN (AC) | 20 | | 2, 6 |
| Low side driver voltage | VLDRV (DC) | –0.3 to +16 | V | 2 |
| | VLDRV (AC) | 20 | | 2, 6 |
| Switch node voltage | VSWH (DC) | 16 | V | 2 |
| | VSWH (AC) | 20 | | 2, 6 |
| BOOT voltage | VBOOT | 22 | V | 2 |
| DISBL# voltage | Vdisble | –0.3 to VCIN | V | 2 |
| PWM voltage | Vpwm | –0.3 to +5.3 | V | 2, 4 |
| | | –0.3 to +0.3 | V | 2, 5 |
| Reg5V current | Ireg5V | –10 to +0.1 | mA | 3 |
| Operating junction temperature | Tj-opr | –40 to +150 | °C | |
| Storage temperature | Tstg | –55 to +150 | °C | |

Notes: 1. Pt(25) represents a PCB temperature of 25°C, and Pt(100) represents 100°C.
2. Rated voltages are relative to voltages on the CGND and PGND pins.
3. For rated current, (+) indicates inflow to the chip and (–) indicates outflow.
4. This rating is when UVL (Under Voltage Lock out) is ineffective (normal operation mode).
5. This rating is when UVL (Under Voltage Lock out) is effective (lock out mode).
6. The specification values indicated “AC” are limited within 100 ns.



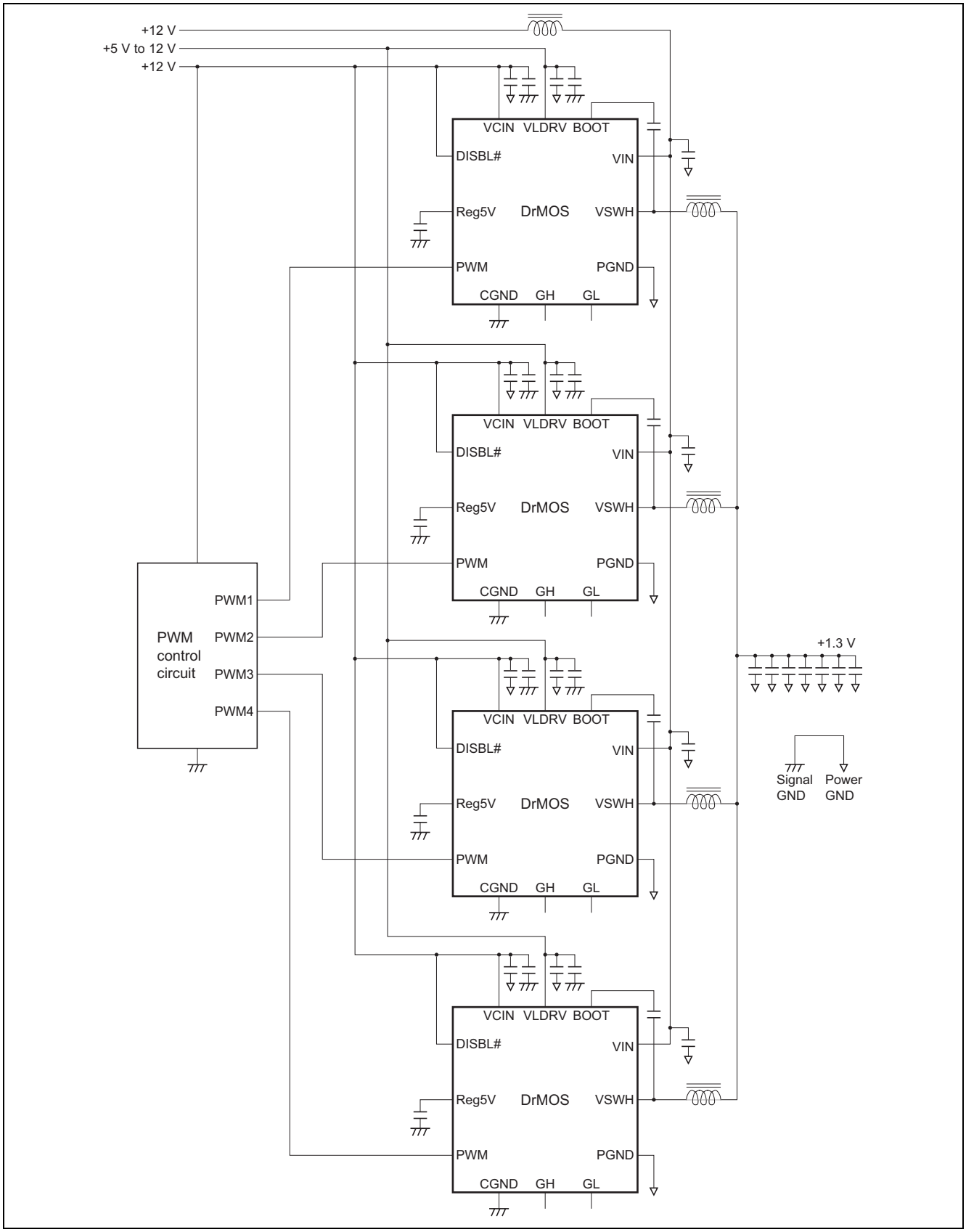
## Electrical Characteristics

(Ta = 25°C, VCIN = 12 V, VLDRV = 5 V, VSWH = 0 V, unless otherwise specified)

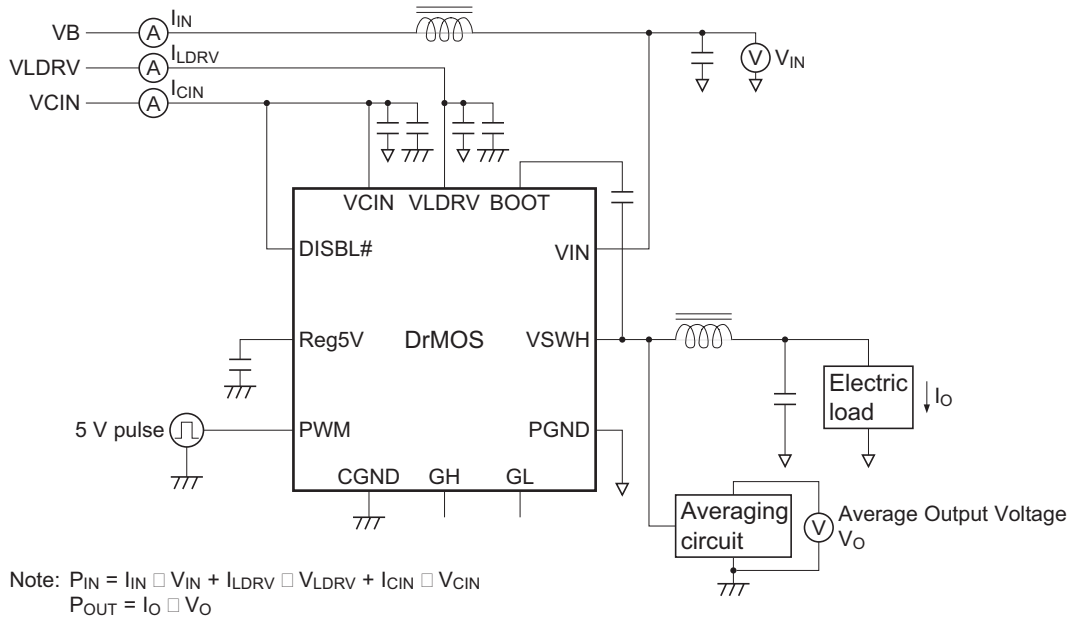
| Item | | Symbol | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| Supply | VCIN start threshold | $V_H$ | 8.1 | 9.0 | 9.9 | V | |
| | VCIN shutdown threshold | $V_L$ | 6.5 | 7.2 | 7.9 | V | |
| | UVLO hysteresis | dUVL | — | 1.8 *1 | — | V | $V_H - V_L$ |
| | VCIN bias current | $I_{CIN}$ | 10.5 | 14.0 | 18.5 | mA | $f_{PWM}$ = 1 MHz, $t_{on\text{-}PWM}$ = 125 ns |
| | VLDRV bias current | $I_{LDRV}$ | 31.5 | 40.7 | 46.5 | mA | $f_{PWM}$ = 1 MHz, $t_{on\text{-}PWM}$ = 125 ns |
| PWM Input | PWM rising threshold | $V_{H\text{-}PWM}$ | 3.5 | 3.8 | 4.1 | V | |
| | PWM falling threshold | $V_{L\text{-}PWM}$ | 0.9 | 1.2 | 1.5 | V | |
| | PWM input resistance | $R_{IN\text{-}PWM}$ | 30 | 50 | 70 | kΩ | PWM = 1 V |
| | Tri-state shutdown window | $V_{IN\text{-}SD}$ | $V_{L\text{-}PWM}$ | — | $V_{H\text{-}PWM}$ | V | |
| | Shutdown hold-off time | $t_{HOLD\text{-}OFF}$ | — | 240 *1 | — | ns | |
| 5V Regulator | Output voltage | Vreg | 4.75 | 5.0 | 5.25 | V | |
| | Line regulation | Vreg-line | –10 | 0 | 10 | mV | VCIN = 12 V to 16 V |
| | Load regulation | Vreg-load | –10 | 0 | 10 | mV | Ireg = 0 to 10 mA |
| DISBL# Input | Disable threshold | $V_{DISBL}$ | 0.9 | 1.2 | 1.5 | V | |
| | Enable threshold | $V_{ENBL}$ | 1.9 | 2.4 | 2.9 | V | |
| | Input current | $I_{DISBL}$ | 0.5 | 2.0 | 5.0 | µA | DISBL# = 1 V |

Note: 1. Reference values for design. Not 100% tested in production.

## Typical Application

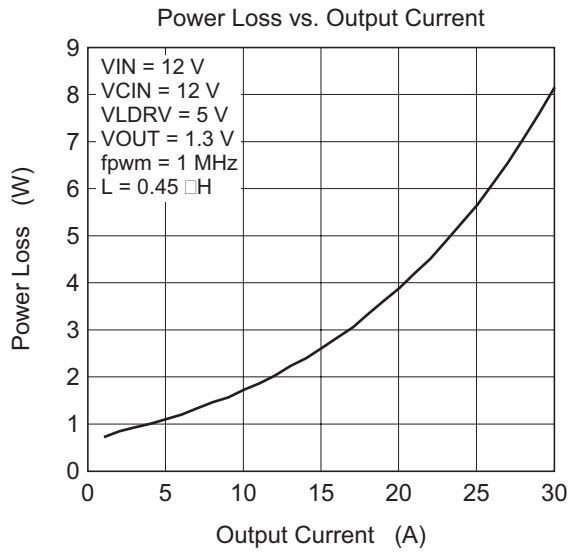


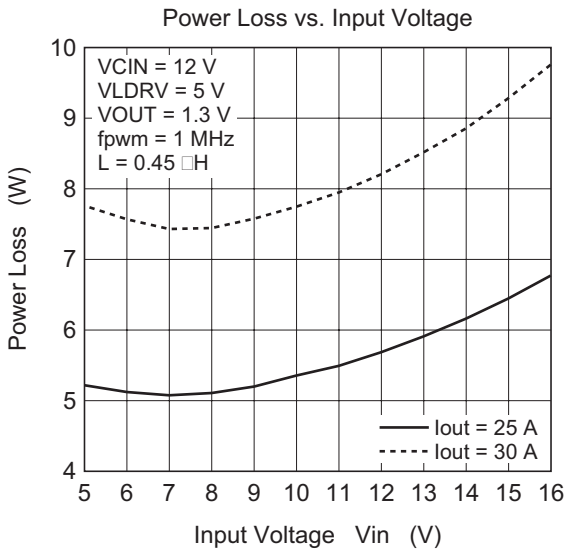
## Test Circuit

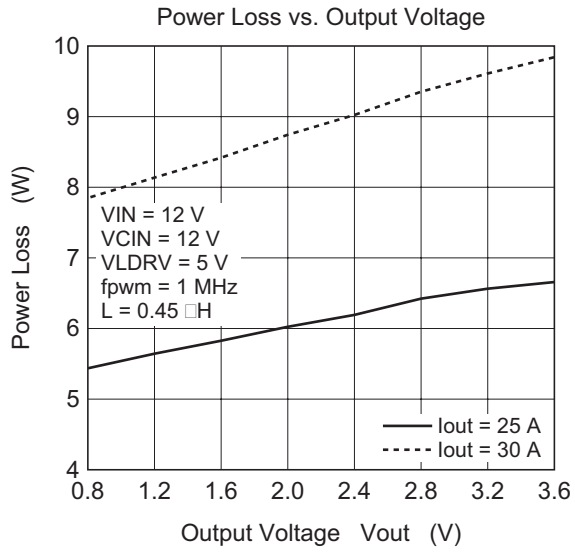


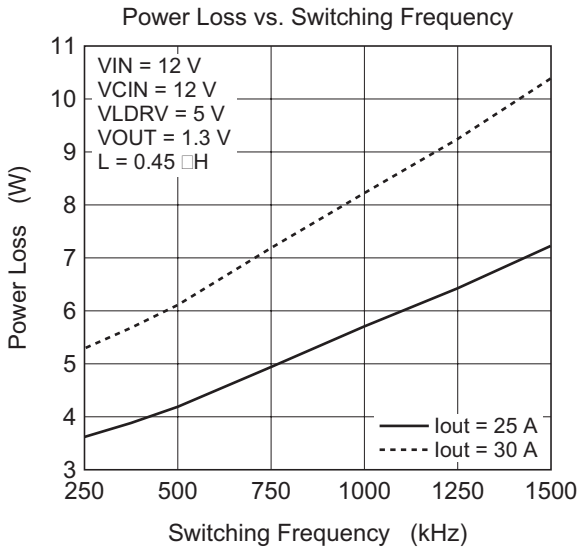

Note: $P_{IN} = I_{IN} \times V_{IN} + I_{LDRV} \times V_{LDRV} + I_{CIN} \times V_{CIN}$
$P_{OUT} = I_O \times V_O$
Efficiency = $P_{OUT} / P_{IN}$
$P_{LOSS}$(DrMOS) = $P_{IN} - P_{OUT}$

## Typical Data

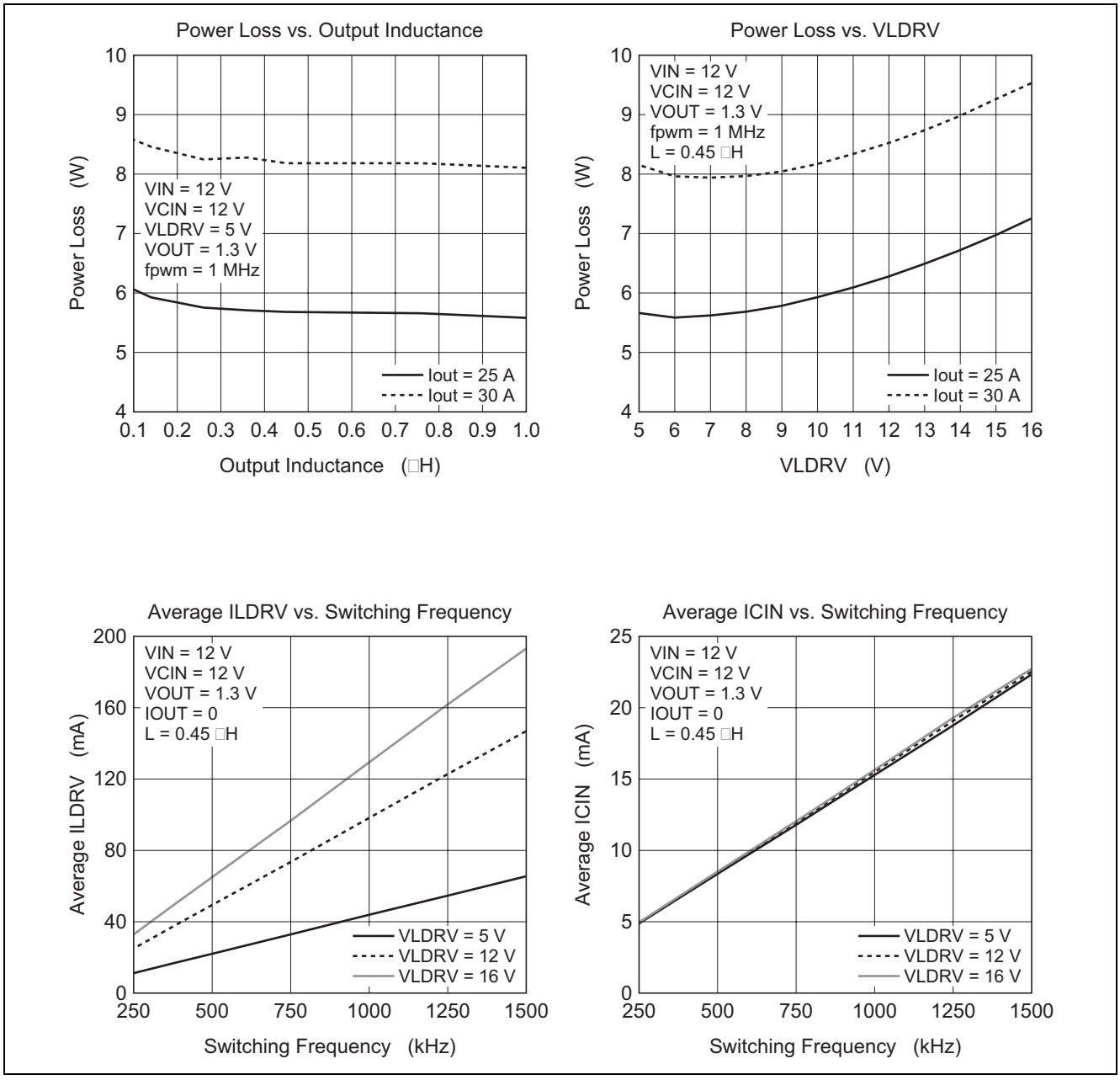


## **Typical Data** (cont.)



## Description of Operation

The DrMOS multi-chip module incorporates a high-side MOS FET, low-side MOS FET, and MOS-FET driver in a single QFN package. Since the parasitic inductance between each chip is extremely small, the module is highly suitable for use in buck converters to be operated at high frequencies. The control timing between the high-side MOS FET, low-side MOS FET, and driver is optimized so that high efficiency can be obtained at low output-voltage.

### Driver

The driver has two types of power-supply voltage input pin, VCIN and VLDRV. VCIN supplies the operating voltage to the internal logic circuit. The low-side driving voltage is applied to VLDRV, so setting of the gate-driving voltage for the low-side MOS FET is independent of the voltage on VCIN. The VLDRV setting voltage is from 5 V to 16 V.

The VCIN pin is connected to the UVL (under-voltage lockout) module, so that the driver is disabled as long as VCIN is 9 V or less. On cancellation of UVL, the driver remains enabled until the UVL input is driven to 7.2 V or less. The signal on pin DISBL# also enables or disables the circuit. When UVL disables the circuit , the built-in 5 V regulator does not operate, but when the signal on DISBL# disables the circuit, only output-pulse generation is terminated, and the 5 V regulator is not disabled.

| VCIN | VLDRV | DISBL# | Reg5V | Driver state |
|---|---|---|---|---|
| L | >5 V | * | 0 | Disable (GL, GH = L) |
| H | >5 V | L | 5 V | Disable (GL, GH = L) |
| H | >5 V | H | 5 V | Active |
| H | >5 V | Open | 5 V | Disable (GL, GH = L) |

Voltages from –0.3 V to VCIN can be applied to the DISBL# pin, so on/off control by a logic IC or the use of a resistor, etc., to pull the DISBL# line up to VCIN are both possible.

The built-in 5 V regulator is a series regulator with temperature compensation. The voltage output by this regulator determines the operating voltage of the internal logic and gate-voltage swing for the high-side MOS FET. A ceramic capacitor with a value of 0.1 µF or more must be connected between the CGND plane and the Reg5V pin.

The PWM pin is the signal input pin for the driver chip. The input-voltage range is –0.3 V to (Reg5V + 3 V). When the PWM input is high, the gate of the high-side MOS FET (GH) is high and the gate of the low-side MOS FET (GL) is low.

| PWM | GH | GL |
|---|---|---|
| L | L | H |
| H | H | L |

The PWM input is TTL level and has hysteresis. When the PWM input signal is abnormal, e.g., when the signal route from the control IC is abnormal, the tri-state function turns off the high- and low-side MOS FETs. This function operates when the PWM input signal stays in the input hysteresis window for 240 ns (typ.). After the tri-state mode has been entered and GH and GL have become low, a PWM input voltage of 3.8 V or more is required to make the circuit return to normal operation.

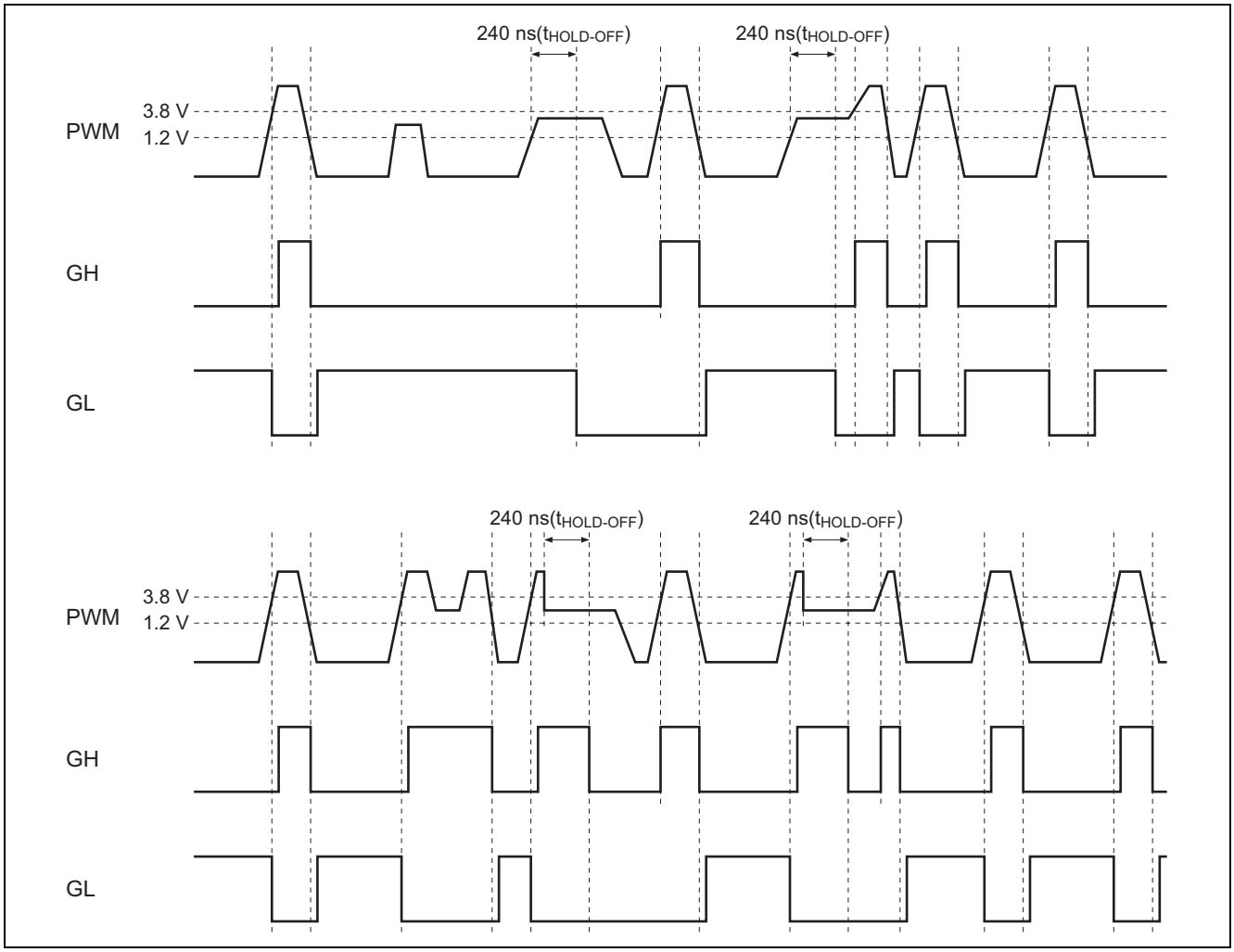



**Figure 1**

The equivalent circuit for the PWM-pin input is shown in the next figure. M1 is in the ON state during normal operation; after the PWM input signal has stayed in the hysteresis window for 240 ns (typ.) and the tri-state detection signal has been driven high, the transistor M1 is turned off. From this circuit configuration, we can see that the voltage on the PWM pin when open-circuit will be about 2.5 V, so the tri-state protection function will operate.

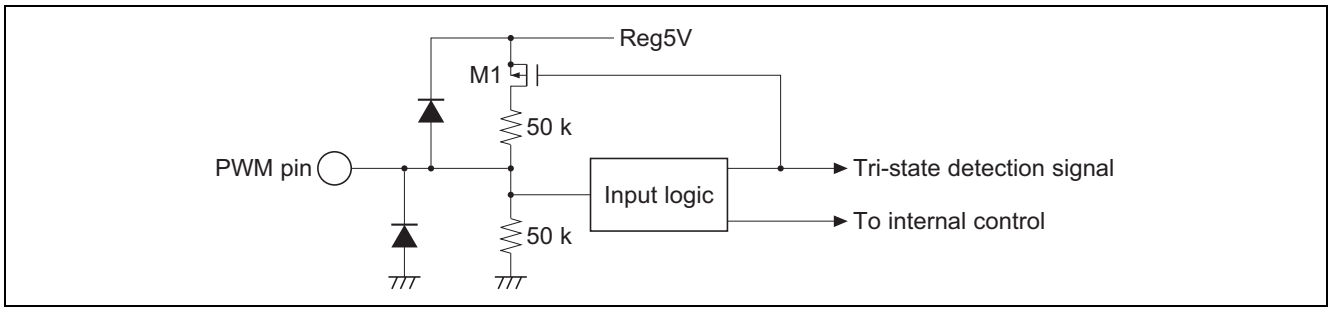



**Figure 2 Equivalent Circuit for the PWM-pin Input**

For the high-side driver, the BOOT pin is the power-supply voltage pin and voltage VSWH provides a standard for operation of the high-side driving circuit. Consequently, the difference between the voltage on the BOOT and VSWH pins becomes the gate swing for the high-side MOS FET. Connect a bootstrap capacitor between the BOOT pin and the VSWH pin. Since the Schottky barrier diode (SBD) is connected between the BOOT and Reg5V pins, this bootstrap capacitor is charged up to 5 V. When the high-side MOS FET is turned on, voltage VSWH becomes equal to VIN, so VBOOT is boosted to VSWH + 5 V.

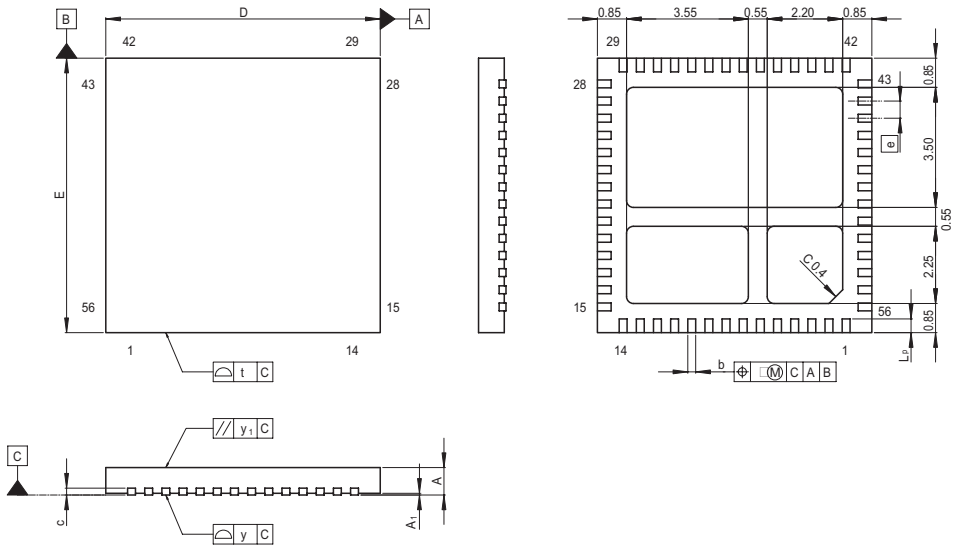
The GH and GL pins are the gate-monitor pins for each MOS FET.

### MOS FETs

The MOS FETs incorporated in R2J20601NP are highly suitable for synchronous-rectification buck conversion. For the high-side MOS FET, the drain is connected to the VIN pin and the source is connected to the VSWH pin. For the low-side MOS FET, the drain is connected to the VSWH pin and the source is connected to the PGND pin.

# Package Dimensions

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-HWQFN56-8x8-0.50 | PWQN0056KA-A | TNP-56TV | 0.17g |




( Ni/Pd/Au plating )

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 7.90 | 8.00 | 8.10 |
| E | 7.90 | 8.00 | 8.10 |
| $A_2$ | — | — | — |
| A | — | — | 0.80 |
| $A_1$ | 0 | — | 0.05 |
| b | 0.18 | 0.23 | 0.28 |
| $b_1$ | — | — | — |
| e | — | 0.50 | — |
| $L_p$ | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.10 |
| y | — | — | 0.08 |
| $y_1$ | — | — | 0.10 |
| t | — | — | 0.15 |
| $H_D$ | — | — | — |
| $H_E$ | — | — | — |
| $Z_D$ | — | — | — |
| $Z_E$ | — | — | — |
| c | — | 0.20 | — |
| $c_1$ | — | — | — |

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Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

**Renesas Technology Malaysia Sdn. Bhd**
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510



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