NEC

MOS INTEGRATED CIRCUIT

μPD9611

FOUR-CHANNEL PCM CODEC

The μPD9611 incorporates 4-channel A-law/μ-law PCM CODECs compliant with ITU-T Recommendation G.711/G.714 and is suitable for applications such as PBX analog subscriber line circuits.

Its gain setting circuit allows transmit/receive gain to be set for 4 channels independently by externally inputting digital signals.

FEATURES

- Single-chip CMOS monolithic LSI
- ITU-T Recommendation G.711/G.714 compliant
- Four-channel PCM CODECs integrated on a single chip
- Compatible with A-law and μ-law
- Digital gain setting for each channel
  - Transmit : +7.5 to –8.0 dB (0.5 dB step)
  - Receive : 0 to –15.5 dB (0.5 dB step)
- Data transfer system: Transmit/receive synchronization
- Data rate: 2048 kHz
- +5 V single power supply
- Power down function for each channel
- Low power consumption

ORDERING INFORMATION

Part Number	Package
μPD9611GT	48-pin shrink SOP (375 mil)

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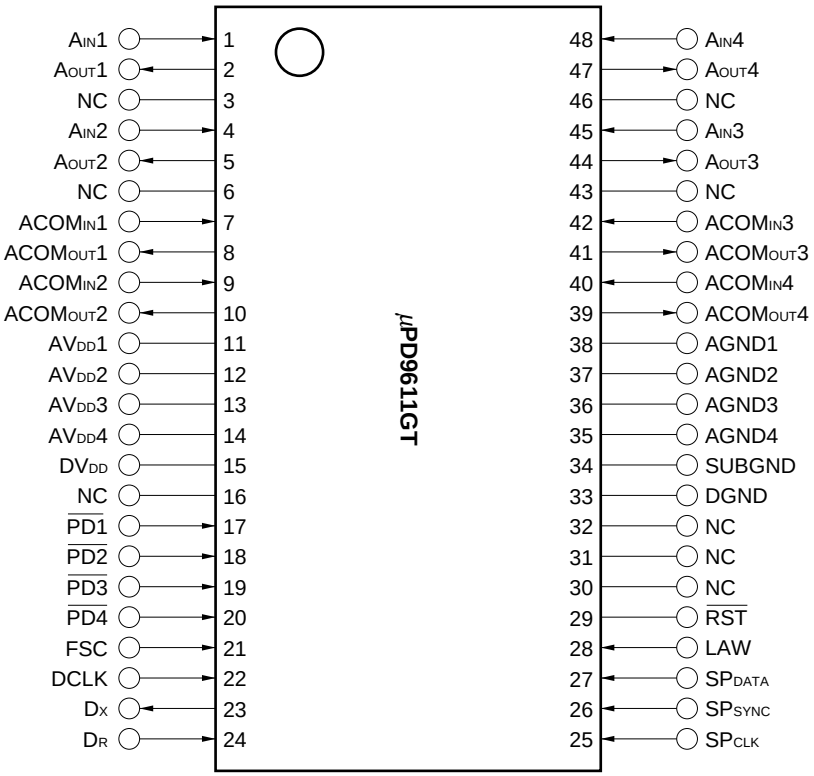
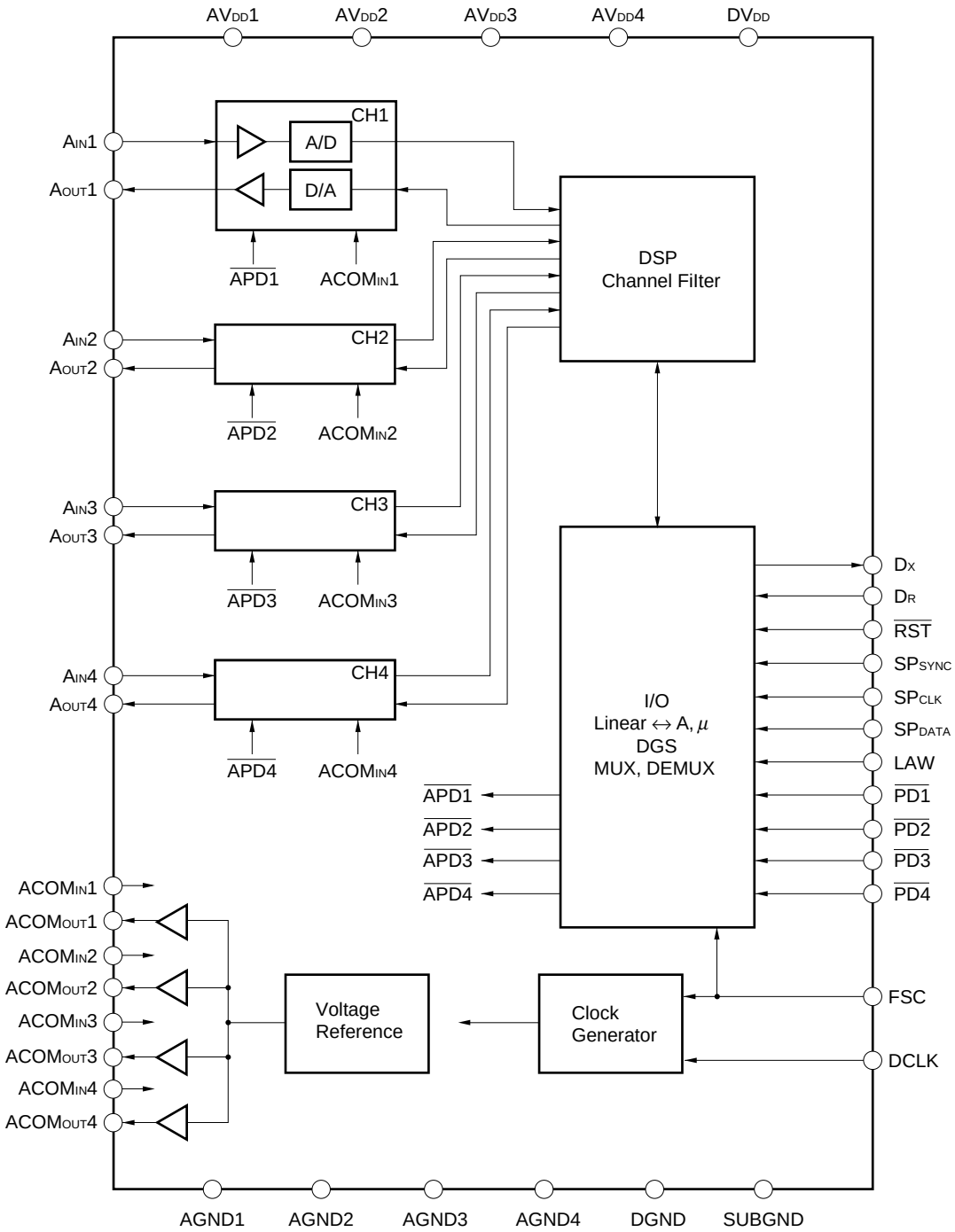
PIN CONFIGURATION (Top View)

48-pin shrink SOP (375 mil)



ACOMIN1-ACOMIN4	: Analog common voltage in	DX	: Transmit PCM data out
ACOMOUT1-ACOMOUT4	: Analog common voltage out	FSC	: Frame synchronous clock in
AGND1-AGND4	: Analog ground	LAW	: A-law/μ-law control in
AIN1-AIN4	: Analog signal in	NC	: No connection
AOUT1-AOUT4	: Analog signal out	$\overline{PD1}$-$\overline{PD4}$	: Power down control
AVDD1-AVDD4	: Analog power supply	$\overline{RST}$	: Reset in
DCLK	: Data clock in	SPCLK	: Serial port data clock in
DGND	: Digital ground	SPDATA	: Serial port data in
DR	: Receive PCM data in	SPSYNC	: Serial port synchronous clock in
DVDD	: Digital power supply	SUBGND	: Sub ground

BLOCK DIAGRAM



1. PIN DESCRIPTION

Pin No.	Symbol	I/O	Name and Function
1	$A_{IN}1$	I	Transmit analog input pin for channel 1 When not used, connect to $ACOM_{OUT}1$ pin.
2	$A_{OUT}1$	O	Receive analog output pin for channel 1
3	NC	–	Leave this pin open.
4	$A_{IN}2$	I	Receive analog input pin for channel 2 When not used, connect to $ACOM_{OUT}1$ pin.
5	$A_{OUT}2$	O	Transmit analog output pin for channel 2
6	NC	–	Leave this pin open.
7	$ACOM_{IN}1$	I	Signal reference voltage input for channel 1
8	$ACOM_{OUT}1$	O	Signal reference voltage output for channel 1
9	$ACOM_{IN}2$	I	Signal reference voltage input for channel 2
10	$ACOM_{OUT}2$	O	Signal reference voltage output for channel 2
11	$AV_{DD}1$	–	Analog power supply pin for channel 1 +5 ± 0.25 V
12	$AV_{DD}2$	–	Analog power supply pin for channel 2 +5 ± 0.25 V
13	$AV_{DD}3$	–	Analog power supply pin for channel 3 +5 ± 0.25 V
14	$AV_{DD}4$	–	Analog power supply pin for channel 4 +5 ± 0.25 V
15	DV_{DD}	–	Digital power supply pin +5 ± 0.25 V
16	NC	–	Leave this pin open.
17	$\overline{PD1}$	I	Power-down control input pin for channel 1 Channel 1 enters power-down mode when this signal is low level. The output of D_X pin for channel 1 becomes high-impedance and $A_{OUT}1$ becomes signal reference voltage in the power-down mode.
18	$\overline{PD2}$	I	Power-down control input pin for channel 2 Channel 2 enters power-down mode when this signal is low level. The output of D_X pin for channel 2 becomes high-impedance and $A_{OUT}2$ becomes signal reference voltage in the power-down mode.
19	$\overline{PD3}$	I	Power-down control input pin for channel 3 Channel 3 enters power-down mode when this signal is low level. The output of D_X pin for channel 3 becomes high-impedance and $A_{OUT}3$ becomes signal reference voltage in the power-down mode.
20	$\overline{PD4}$	I	Power-down control input pin for channel 4 Channel 4 enters power-down mode when this signal is low level. The output of D_X pin for channel 4 becomes high-impedance and $A_{OUT}4$ becomes signal reference voltage in the power-down mode.
21	FSC	I	Frame synchronous clock input pin (8 kHz)
22	DCLK	I	Data clock input pin (2048 kHz)
23	D_X	O	Transmit PCM data output pin This pin outputs PCM data for channel 1 to 4 in synchronization with rising edges of DCLK after rising edges of FSC. It becomes high-impedance for other timings.
24	D_R	I	Receive PCM data input pin This pin inputs PCM data for channel 1 to 4 in synchronization with falling edges of DCLK after rising edges of FSC.
25	SP_{CLK}	I	Setting data clock input pin
26	SP_{SYNC}	I	Setting synchronous clock input pin
27	SP_{DATA}	I	Setting data input pin

Pin No.	Symbol	I/O	Name and Function
28	LAW	I	A-law/μ-law select pin in common to four channels L: A-law, H: μ-law
29	$\overline{RST}$	–	Reset input, power-on reset pin H: normal operation L : internal registers are in the default status.
30-32	NC	–	Leave this pin open.
33	DGND	–	Digital ground pin
34	SUBGND	–	Substrate ground pin
35	AGND4	–	Analog ground pin for channel 4
36	AGND3	–	Analog ground pin for channel 3
37	AGND2	–	Analog ground pin for channel 2
38	AGND1	–	Analog ground pin for channel 1
39	$ACOM_{OUT}4$	O	Signal reference voltage output for channel 4
40	$ACOM_{IN}4$	I	Signal reference voltage input for channel 4
41	$ACOM_{OUT}3$	O	Signal reference voltage output for channel 3
42	$ACOM_{IN}3$	I	Signal reference voltage input for channel 3
43	NC	–	Leave this pin open.
44	$A_{OUT}3$	O	Receive analog output pin for channel 3
45	$A_{IN}3$	I	Transmit analog input pin for channel 3 When not used, connect to $ACOM_{OUT}1$ pin.
46	NC	–	Leave this pin open.
47	$A_{OUT}4$	O	Receive analog output pin for channel 4
48	$A_{IN}4$	I	Transmit analog input pin for channel 4 When not used, connect to $ACOM_{OUT}1$ pin.

2. CAUTIONS ON USE

(1) Absolute maximum ratings

Application of voltage or current in excess of the absolute maximum ratings to the μPD9611 may result in damage due to latch up, etc. Be especially cautions about power supply noise, etc.

(2) Wiring pattern

The design of the ground pattern is extremely important for operating the μPD9611 with high precision. Connect the analog ground pins (AGND1 to AGND4), digital ground pin (DGND) and substrate ground pin (SUBGND) close to the IC pins, and connect to a wide analog ground line on the board.

(3) Addition of bypass capacitors for power supply pins

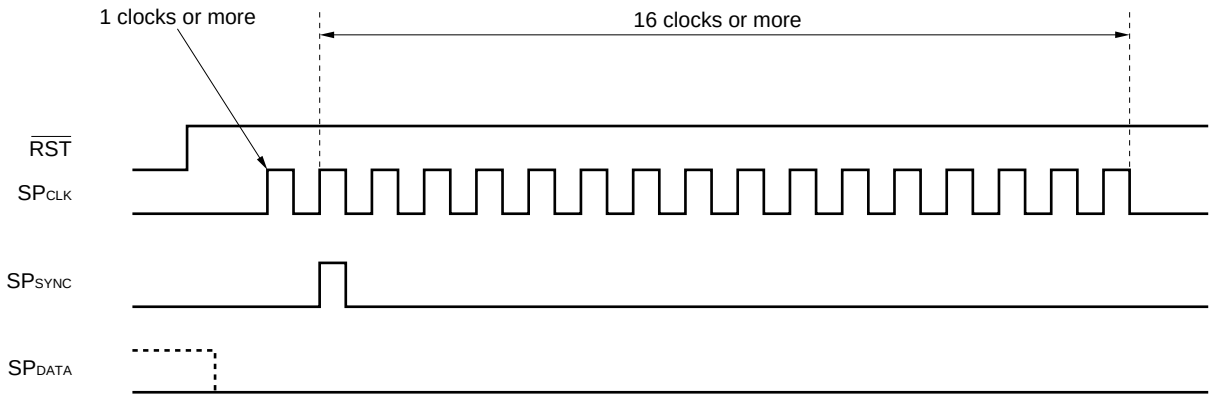
Because the μPD9611 uses many internal high-frequency operational amplifiers, high power supply impedance can cause instability (such as oscillation) in these internal operational amplifiers. To suppress such instability and eliminate power supply noise, connect all power supply pins ($AV_{DD}1$ to $AV_{DD}4$, DV_{DD}) close to the IC pins, and put bypass capacitors (C_{VDD} = approximately 0.1 μF) having superior high-frequency characteristics very close to the pins.

(4) Addition of bypass capacitors for ACOM pins

The μPD9611 incorporates references voltages for signal sources. Superposing of noise on these reference voltages may have adverse effects on transmission characteristics, etc. Therefore, connect the $ACOM_{OUT}$ pin and $ACOM_{IN}$ pin close to the IC pins, and put bypass capacitors (C_{ACOM} = approximately 0.1 μF) having superior high-frequency characteristics very close to the pins.

(5) Control or SP_{DATA} pin on reset

When inputting the setting data from the SP_{DATA} pin after the μPD9611 is reset, first input the following patterns to reset to 0 the couter used to fetch data from the SP_{DATA} pin.



After ther $\overline{RST}$ pin has been set to the high level, input 1 clock or more to the SP_{CLK} pin, set the SP_{SYNC} pin to the high level and input 16 clocks more to the SP_{CLK} pin.
During this operation, the SP_{DATA} pin is held at the low level. Afterwards, input the setting data.

3. GENERAL OPERATION

(1) PCM data transfer

In the transmit section, if FSC pin is set to the high level in synchronization with the rising edge (↑) of the data clock applied to the DCLK pin, the D_X pin becomes active and sign bit data (MSB) of channel 1 is output. The following data of 7 bits is clocked out in synchronization with the rising edge (↑) of each data clock. Sign bit data (MSB) of channel 2 is output in synchronization with the rising edge (↑) of the 9th data clock. In the same manner, each data up to channel 4 is output and the rising edge (↑) of the 33rd data clock then sets the D_X pin to high-impedance state.
Similarly, in the receive section, if the FSC pin is set to the high level in synchronization with the rising edge (↑) of the data clock applied to the DCLK pin, data of D_R pin is latched by the falling edges (↓) of the data clock and consecutively clocked in.

(2) Power down control

The μPD9611 has the following two methods for power down control and is able to control power-down independently for each channel.

- Sets pins $\overline{PD1}$ to $\overline{PD4}$ to high or low level.
- Inputs 8-bit setting data from SP_{DATA} pin (see **(5) Control of SP_{DATA} pin**).

Internal data is the logical sum of $\overline{PD1}$ to $\overline{PD4}$ pin state and 8-bit setting data input.
If the internal data is 0, the channel enters the power-down state. If the internal data is 1, the channel enters the power-up state. In the power down state, PCM data in the channel goes to high-impedance state and analog output becomes the signal reference voltage level.

8-Bit Setting Data (Channel 1)	$\overline{PD1}$ Pin	Internal Data
0	0	0
1	0	1
0	1	1
1	1	1

Remarks 1. 0: Power down, 1: Power up

2. The settings are the same for channel 2 to channel 4.

(3) A-law/μ-law control

The μPD9611 has the following two methods for A-law/μ-law control.

- Sets LAW pin to high or low level.
- Inputs 8-bit setting data from SP_{DATA} pin (see **(5) Control of SP_{DATA} pin**).

Internal data is the logical sum of LAW pin state and 8-bit setting data input.
If the internal data is 0, the μPD9611 enters A-law mode. If the internal data is 1, the μPD9611 enters μ-law mode.

8-Bit Setting Data	LAW Pin	Internal Data
0	0	0
1	0	1
0	1	1
1	1	1

Remark 0: A-law, 1: μ-law

(4) Gain Setting control for transmit/receive

The μPD9611 can control gain settings independently for the transmit/receive by inputting 8-bit setting data (see **(5) Control of SP_{DATA} pin**) from the SP_{DATA} pin for four channels. Gain can be set from +7.5 to –8.0 dB for the transmit and +0.0 dB t o –15.5 dB for the receive in 0.5 dB steps.
8-bit setting data input from SP_{DATA} pin specifies the channel set in the first 8 bits, and performs selection of transmit/receive and gain setting in the second 8 bits.

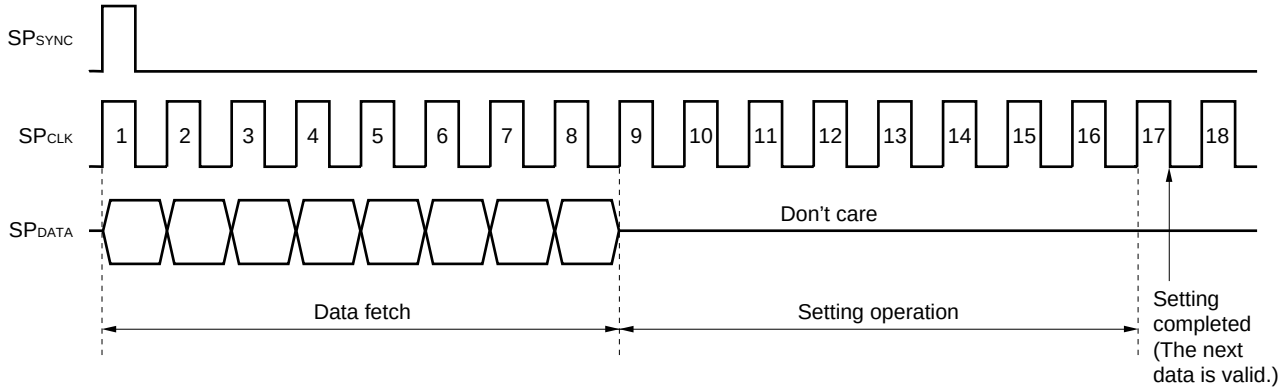
(5) Control of SP_{DATA} pin

If SP_{SYNC} pin is set to the high level in synchronization with the rising edge (↑) of the data clock applied to the SP_{CLK} pin, data of the SP_{DATA} pin is latched by the falling edge (↓) of the data clock and consecutively fetched in.

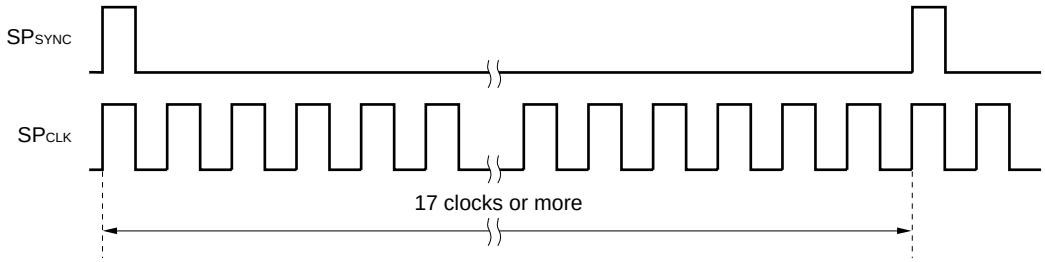
After the 8-bit data has been fetched, the setting operation is performed according to the data.

This setting operation is performed during the 8 clocks after fetching the data and the next data is valid at the 17th clock.

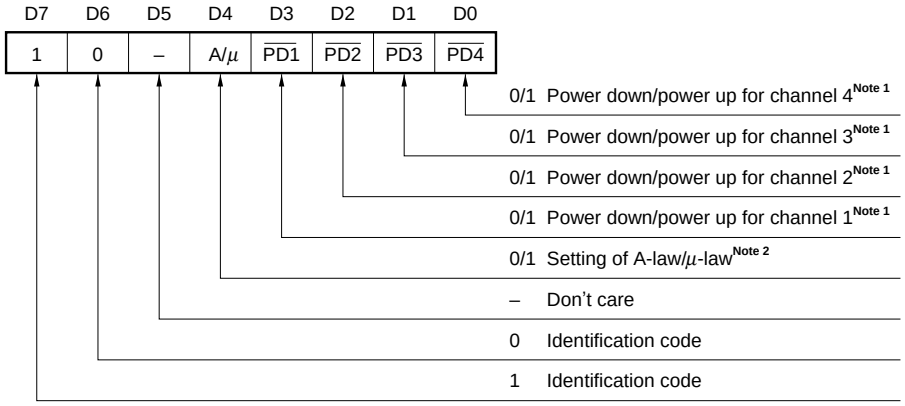
Therefore, when setting 1 word (8 bits) of data, input 17 clocks or more to the SP_{CLK} pin.



Ensure that 17 clocks or more are input to the SP_{CLK} pin between the rising of SP_{SYNC} and the rising of the next SP_{SYNC}.



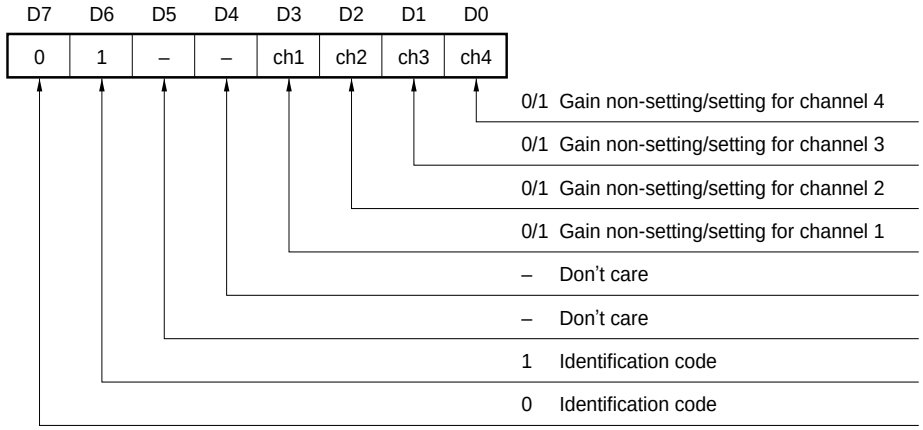
- **A/μ-law, power down control**



Notes 1. Default setting is power down mode.

2. Default setting is A-law mode.

- **Transmit/receive gain setting control (1st word)**



Transmit/receive gain setting control (2nd word)

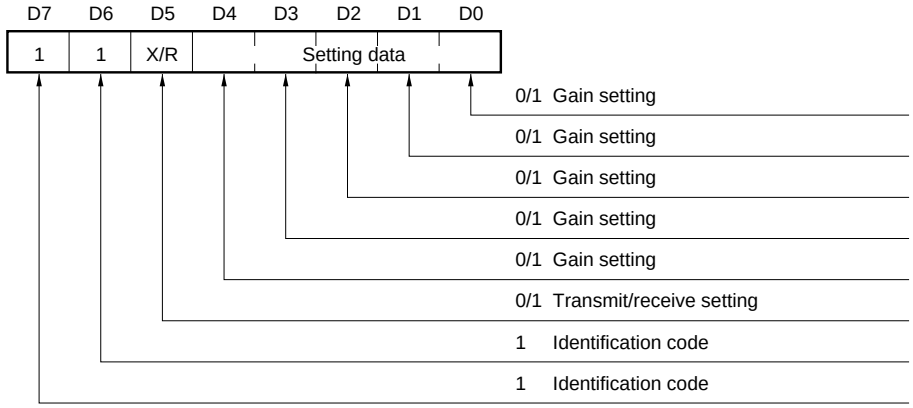


Table of Gain Setting Codes

(1/2)

Setting Item	Setting Level	1st Word								2nd Word							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Gain setting for transmit	+7.5 dB	0	1	–	–	ch1	ch2	ch3	ch4	1	1	0	1	0	0	0	0
	+7.0 dB									1	1	0	1	0	0	0	1
	+6.5 dB									1	1	0	1	0	0	1	0
	+6.0 dB									1	1	0	1	0	0	1	1
	+5.5 dB									1	1	0	1	0	1	0	0
	+5.0 dB									1	1	0	1	0	1	0	1
	+4.5 dB									1	1	0	1	0	1	1	0
	+4.0 dB									1	1	0	1	0	1	1	1
	+3.5 dB									1	1	0	1	1	0	0	0
	+3.0 dB									1	1	0	1	1	0	0	1
	+2.5 dB									1	1	0	1	1	0	1	0
	+2.0 dB									1	1	0	1	1	0	1	1
	+1.5 dB									1	1	0	1	1	1	0	0
	+1.0 dB									1	1	0	1	1	1	0	1
	+0.5 dB									1	1	0	1	1	1	1	0
	0.0 dB[Note]									1	1	0	1	1	1	1	1
	–0.5 dB									1	1	0	0	0	0	0	0
	–1.0 dB									1	1	0	0	0	0	0	1
	–1.5 dB									1	1	0	0	0	0	1	0
	–2.0 dB									1	1	0	0	0	0	1	1
	–2.5 dB									1	1	0	0	0	1	0	0
	–3.0 dB									1	1	0	0	0	1	0	1
	–3.5 dB									1	1	0	0	0	1	1	0
	–4.0 dB									1	1	0	0	0	1	1	1
	–4.5 dB									1	1	0	0	1	0	0	0
	–5.0 dB									1	1	0	0	1	0	0	1
	–5.5 dB									1	1	0	0	1	0	1	0
	–6.0 dB									1	1	0	0	1	0	1	1
	–6.5 dB									1	1	0	0	1	1	0	0
	–7.0 dB									1	1	0	0	1	1	0	1
	–7.5 dB									1	1	0	0	1	1	1	0
	–8.0 dB									1	1	0	0	1	1	1	1

Note Default setting

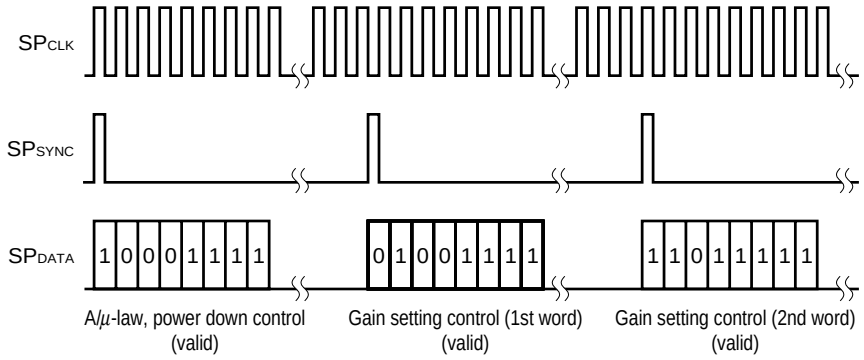
(2/2)

Setting Item	Setting Level	1st Word								2nd Word							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Gain setting for receive	0.0 dB[Note]	0	1	–	–	ch1	ch2	ch3	ch4	1	1	1	1	1	1	1	1
	–0.5 dB									1	1	1	1	1	1	1	0
	–1.0 dB									1	1	1	1	1	1	0	1
	–1.5 dB									1	1	1	1	1	1	0	0
	–2.0 dB									1	1	1	1	1	0	1	1
	–2.5 dB									1	1	1	1	1	0	1	0
	–3.0 dB									1	1	1	1	1	0	0	1
	–3.5 dB									1	1	1	1	1	0	0	0
	–4.0 dB									1	1	1	1	0	1	1	1
	–4.5 dB									1	1	1	1	0	1	1	0
	–5.0 dB									1	1	1	1	0	1	0	1
	–5.5 dB									1	1	1	1	0	1	0	0
	–6.0 dB									1	1	1	1	0	0	1	1
	–6.5 dB									1	1	1	1	0	0	1	0
	–7.0 dB									1	1	1	1	0	0	0	1
	–7.5 dB									1	1	1	1	0	0	0	0
	–8.0 dB									1	1	1	0	1	1	1	1
	–8.5 dB									1	1	1	0	1	1	1	0
	–9.0 dB									1	1	1	0	1	1	0	1
	–9.5 dB									1	1	1	0	1	1	0	0
	–10.0 dB									1	1	1	0	1	0	1	1
	–10.5 dB									1	1	1	0	1	0	1	0
	–11.0 dB									1	1	1	0	1	0	0	1
	–11.5 dB									1	1	1	0	1	0	0	0
	–12.0 dB									1	1	1	0	0	1	1	1
	–12.5 dB									1	1	1	0	0	1	1	0
	–13.0 dB									1	1	1	0	0	1	0	1
	–13.5 dB									1	1	1	0	0	1	0	0
	–14.0 dB									1	1	1	0	0	0	1	1
	–14.5 dB									1	1	1	0	0	0	1	0
	–15.0 dB									1	1	1	0	0	0	0	1
	–15.5 dB									1	1	1	0	0	0	0	0

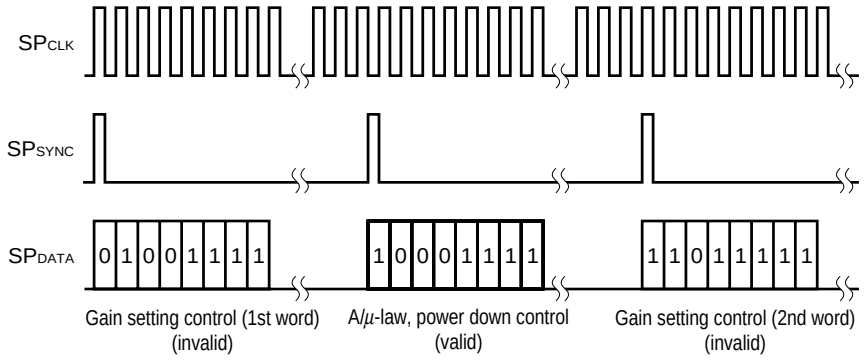
Note Default setting

Gain setting control is set by inputting 8-bit data fo the 1st word first and inputting 8-bit data of the 2nd word in synchronization with the next rising edge of SP_{SYNC}. However, if data other than the identification code of the 2nd word is input after the input of the 1st word, the contents of the 1st word are ignored.

(i) When gain setting control is valid

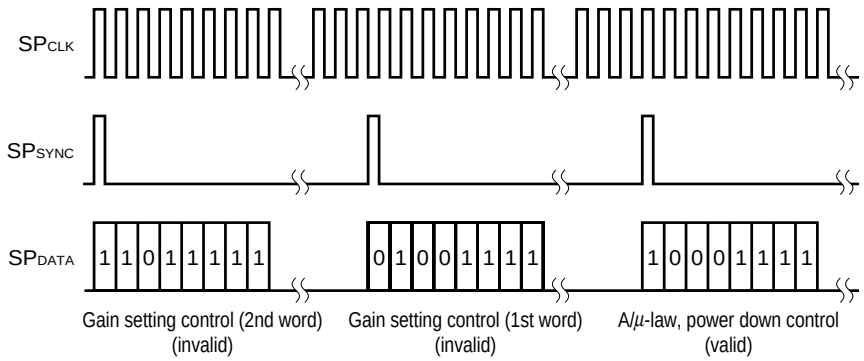


(ii) When gain setting control is invalid –1



Remark Because A/μ-law, power down control is input after input of gain setting control (1st word), gain setting control (1st word) becomes invalid and gain setting control (2nd word) also becomes invalid.

(iii) When gain setting control is invalid –2



Remark Because gain setting control (2nd word) is input before gain setting control (1st word), gain setting control (1st word) becomes invalid. Then, because A/μ-law, power down control is input even if gain setting control (1st word) is input, gain setting control (1st word) becomes invalid.

4. ELECTRICAL SPECIFICATIONS (PRELIMINARY)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	$AV_{DD}1$, $AV_{DD}2$, $AV_{DD}3$, $AV_{DD}4$, DV_{DD}	–0.3 to +7.0	V
Analog input voltage	V_{AIN}	$A_{IN}1$, $A_{IN}2$, $A_{IN}3$, $A_{IN}4$, $ACOM_{IN}1$, $ACOM_{IN}2$, $ACOM_{IN}3$, $ACOM_{IN}4$	–0.3 to V_{DD} +0.3	
Digital input voltage	V_{DIN}	D_R, DCLR, FSC, LAW, $\overline{PD1}$, $\overline{PD2}$, $\overline{PD3}$, $\overline{PD4}$, SP_{CLK}, SP_{SYNC}, SP_{DATA}, $\overline{RST}$	–0.3 to V_{DD} +0.3	
Voltage applied to analog output pin	V_{AOUT}	$A_{OUT}1$, $A_{OUT}2$, $A_{OUT}3$, $A_{OUT}4$, $ACOM_{OUT}1$, $ACOM_{OUT}2$, $ACOM_{OUT}3$, $ACOM_{OUT}4$	–0.3 to V_{DD} +0.3	
Voltage applied to digital output pin	V_{DOUT}	D_X	–0.3 to V_{DD} +0.3	
Power dissipation	P_T		500	mW
Ambient operating temperature	T_A		–20 to +85	°C
Storage temperature	T_{stg}		–65 to +150	

Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

RECOMMENDED OPERATION CONDITIONS (T_A = –20 to +85 °C, V_{DD} = 5 V ± 5 %, GND = 0 V, f_{DCLK} = 2048 kHz)

(1) DC condition

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Ambient operating temperature	T_A		–20	+25	+85	°C
Supply voltage	V_{DD}	$AV_{DD}1$, $AV_{DD}2$, $AV_{DD}3$, $AV_{DD}4$, DV_{DD}	4.75	5.0	5.25	V
Analog input voltage	V_{AI}	$A_{IN}1$, $A_{IN}2$, $A_{IN}3$, $A_{IN}4$ (ACOM as reference)	–1.0		+1.0	
Analog output load resistance	R_{LOAD}	$A_{OUT}1$, $A_{OUT}2$, $A_{OUT}3$, $A_{OUT}4$	50			kΩ
Analog output load capacitance	C_{LOAD}				50	pF
High level input voltage	V_{IH1}	D_R, DCLK, FSC, LAW, $\overline{PD1}$, $\overline{PD2}$, $\overline{PD3}$, $\overline{PD4}$, SP_{CLK}, SP_{SYNC}, SP_{DATA}	2.0		V_{DD}	V
	V_{IH2}	$\overline{RST}$	0.8×V_{DD}		V_{DD}	
Low level input voltage	V_{IL1}	D_R, DCLK, FSC, LAW, $\overline{PD1}$, $\overline{PD2}$, $\overline{PD3}$, $\overline{PD4}$, SP_{CLK}, SP_{SYNC}, SP_{DATA}	0		0.8	
	V_{IL2}	$\overline{RST}$	0		0.2×V_{DD}	

(2) AC condition

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Data clock frequency	f_{CLK}	(= $1/t_{CY}$) ±50 ppm		2048		kHz
Data clock pulse width	t_{CLK}		200			ns
Frame synchronous clock frequency	fs	±50 ppm		8.0		kHz
High level frame synchronous pulse width	t_{WHS}		200			ns
Low level frame synchronous pulse width	t_{WLS}		8			μs
Clock rise time	t_R				50	ns
Clock fall time	t_F				50	ns
Float in synchronous timing	t_{CSD1}				100	ns
	t_{CSD2}		40			ns
Frame synchronous clock and data clock high level width	t_{WHSC}		100			ns
D_R setup time	t_{DSR}	**Note**	65			ns
D_R hold time	t_{DHR}	**Note**	120			ns
SP_{DATA} clock frequency	f_{SPCLK}				2048	kHz
SP_{DATA} setup time	t_{GSR}	**Note**	100			ns
SP_{DATA} hold time	t_{GHR}	**Note**	100			ns
Float in SP synchronous timing	t_{FSD}		40			ns

Note Set the rise time and fall time of the digital input waveform and clock signal used for measuring timings to 5 ns.

DC CHARACTERISTICS

(T_A = –20 to +85 °C, V_{DD} = 5 ± 0.25 V, GND = 0 V, f_{DCLK} = 2048 kHz, and all output pins are unloaded.)

(1) Power consumption

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Circuit current	I_{DD}	All channels in normal operation		23	30	mA
Power-down circuit current	I_{DDPD}	All channels in power-down mode		5	6	

(2) Digital interface

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Digital input current	I_{ID}	D_R, DCLK, FSC, LAW, $\overline{PD1}$, $\overline{PD2}$, $\overline{PD3}$, $\overline{PD4}$, SP_{CLK}, SP_{SYNC}, SP_{DATA}, $\overline{RST}$ Each pin $0 \le V_{DIN} \le V_{DD}$	–10		+10	μA
3-state leakage current	I_L	D_X pin $0 \le V_{DIN} \le V_{DD}$	–10		+10	
High level output voltage	V_{OH}	D_X pin I_{OH} = –150 μA	V_{DD}–0.3			V
Low level output voltage	V_{OL}	D_X pin I_{OL} = 0.8 mA			0.4	
Digital output pin output capacitance	C_{OD}	f = 1 MHz, 0 V other than unmeasured pins			15	pF
Digital input pin input capacitance	C_{ID}	f = 1 MHz, 0 V other than unmeasured pins			10	

(3) Transmit amplifier ($A_{IN}1$, $A_{IN}2$, $A_{IN}3$, $A_{IN}4$ pins)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input bias current	I_B		–10		+10	μA
Input resistance	R_{IN}		1			MΩ
Input capacitance	C_{IN}				10	pF

(4) Receive power amplifier ($A_{OUT}1$, $A_{OUT}2$, $A_{OUT}3$, $A_{OUT}4$ pins)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output offset voltage	V_{OA}	D_R = +0 code ACOM as reference	–50		+50	mV
Maximum output voltage	V_{OM}	ACOM as reference	–1.02		+1.02	V
Output resistance	R_{OUT}			1		Ω

(5) Signal reference voltage output ($ACOM_{OUT}1$, $ACOM_{OUT}2$, $ACOM_{OUT}3$, $ACOM_{OUT}4$ pins)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage	V_{ACOM}		2.35	2.4	2.45	V

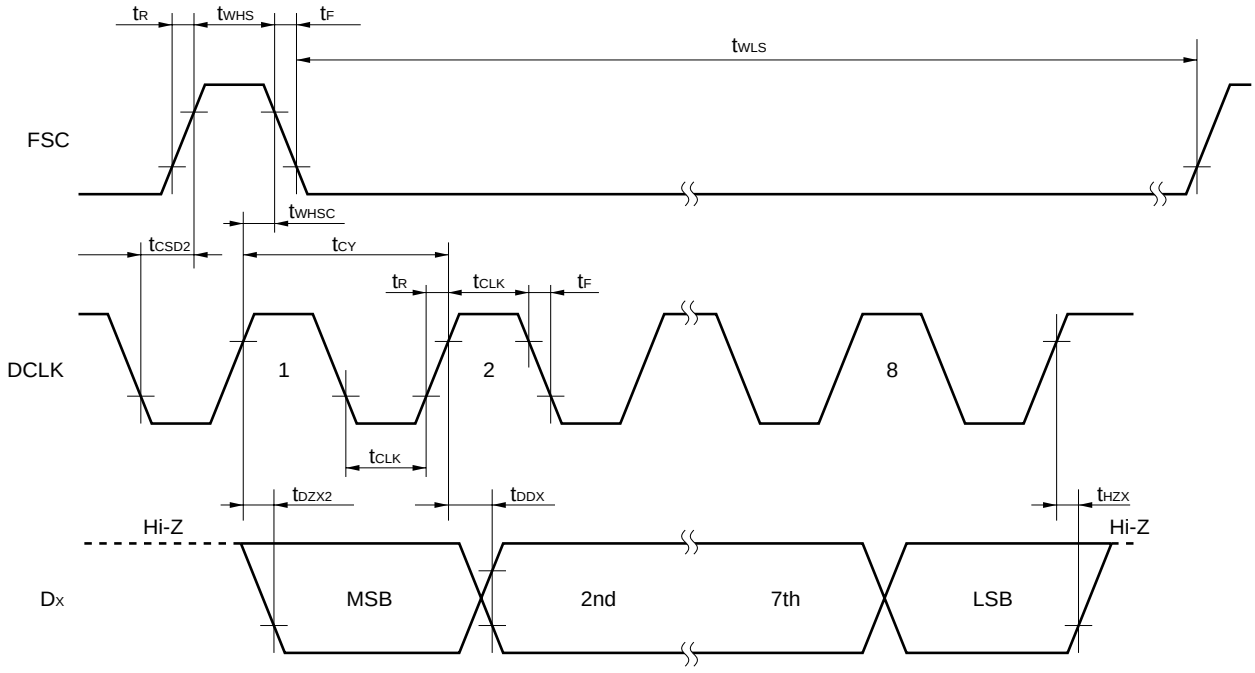
AC CHARACTERISTICS (T_A = –20 to +85 °C, V_{DD} = 5 ± 0.25 V, GND = 0 V, f_{DCLK} = 2048 kHz)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Data enable delay time	t_{DZX1}	D_X when FSC is behind DCLK			100	ns
	t_{DZX2}	D_X when FSC is ahead of DCLK			100	ns
Data delay time	t_{DDX}	D_X pin			100	ns
Data hold time	t_{HZX}	D_X pin		25		ns

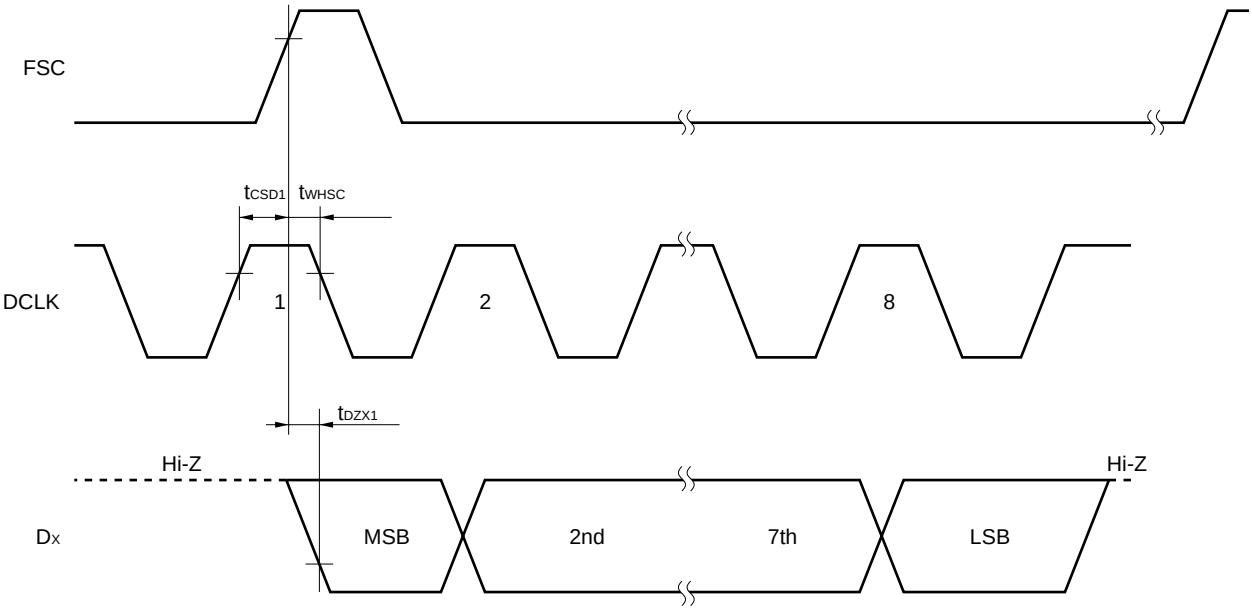
TIMING CHARTS

(1) Transmit timing

(a) When FSC is ahead of DCLK

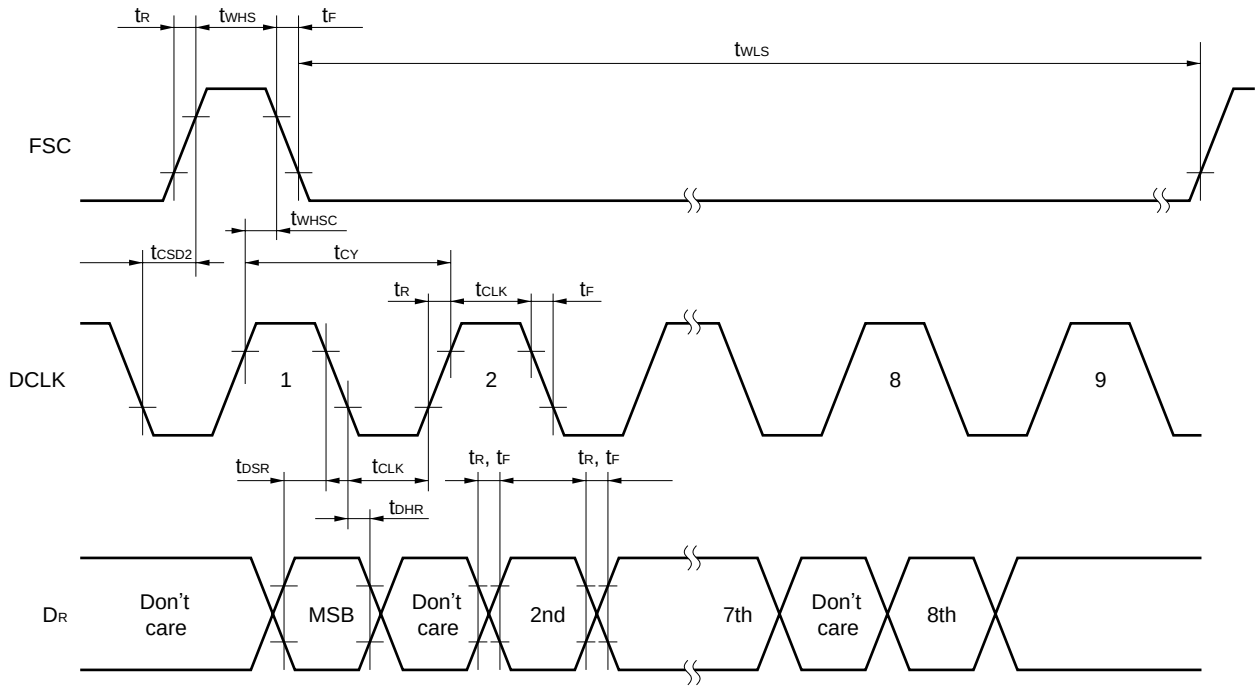


(b) When FSC is behind DCLK

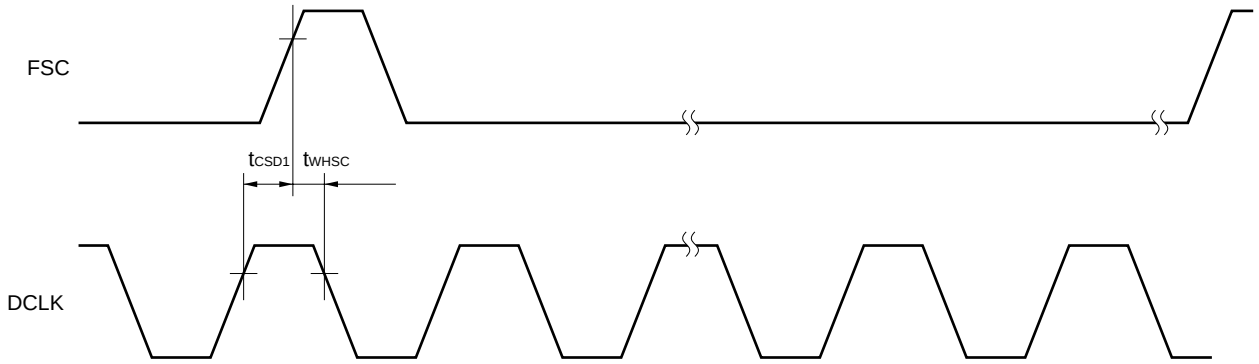


(2) Receive timing

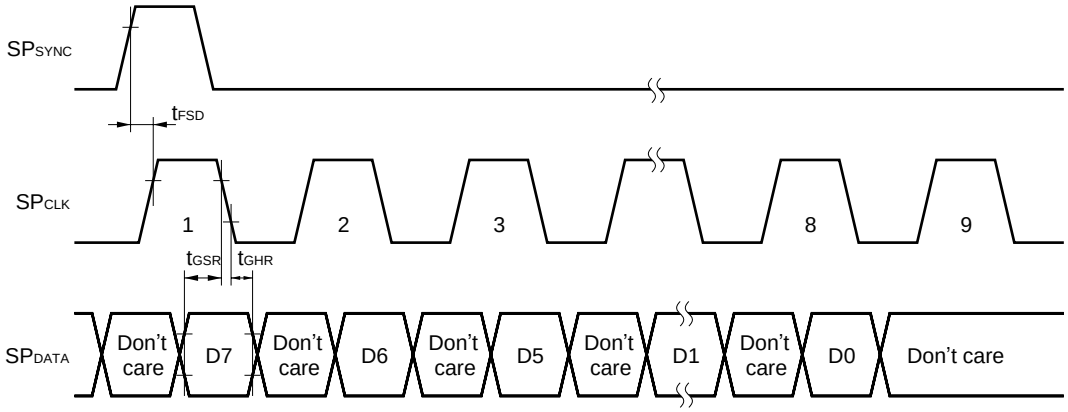
(a) When FSC is ahead of DCLK



(b) When FSC is behind DCLK

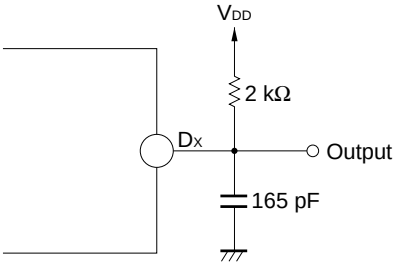


(3) Gain setting timing

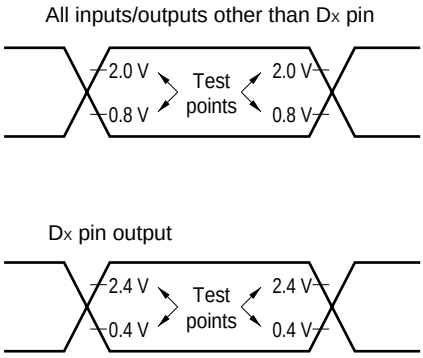


Remark The relationship between SP_{SYNC} and SP_{CLK} is the same as in the receive timing.

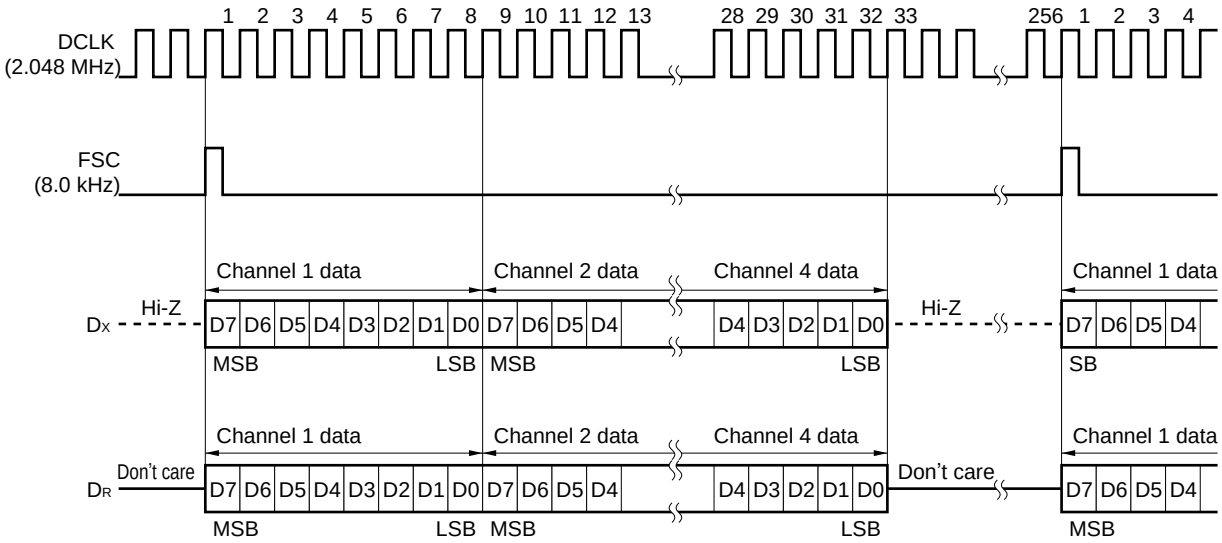
D_X output measuring circuit



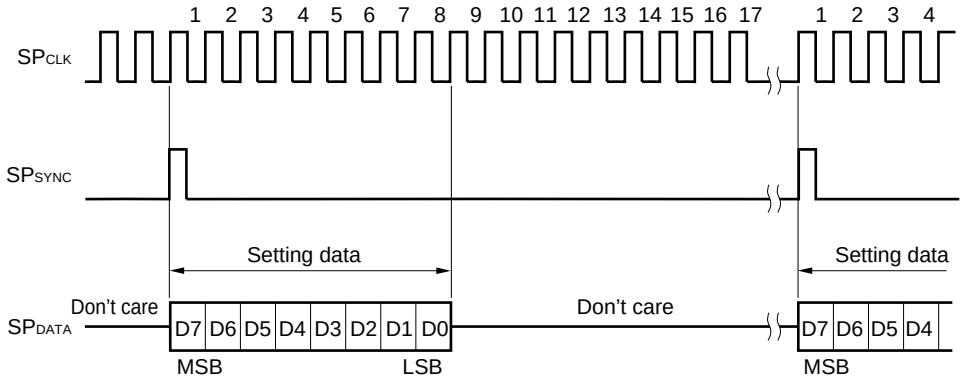
Timing test waveform



(4) Transmit, receive PCM data input/output timing charts



(5) Setting data input timing



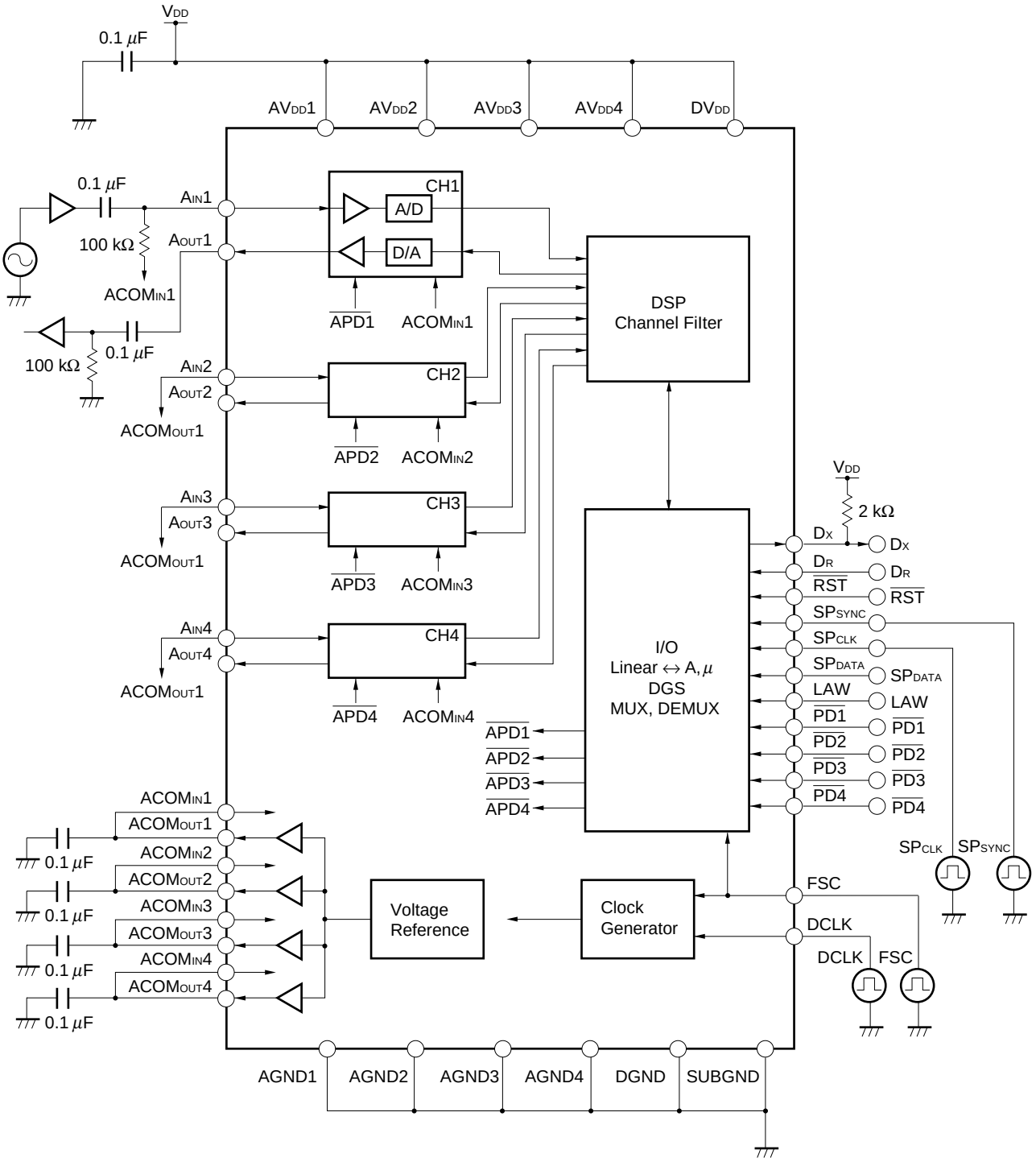
TRANSMISSION CHARACTERISTICS (T_A = –20 to +85 °C, V_{DD} = 5 ± 0.25 V, GND = 0 V, f_{DCLK} = 2048 kHz)

Item	Symbol	Condition	Setting Value	Unit
Zero transmission level point (transmit)	$OTLP_X$	Referenced to 600 Ω	–3.8	dBm
Zero transmission level point (receive)	$OTLP_X$	Referenced to 600 Ω	–3.8	dBm

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Insertion loss	IL	A/D input signal 0 dBm0 1 kHz		–0.3		+0.3	dB
		D/A input signal 0 dBm0 1 kHz		–0.3		+0.3	
Transmission loss frequency characteristics	F_{RX}	A/D Reference input signal 1015 Hz 0 dBm0	60 Hz	24.0		–	dB
			200 Hz	0		2.0	
			300 to 3000 Hz	–0.15		+0.15	
			3200 Hz	–0.15		+0.65	
			3400 Hz	0		0.8	
			3780 Hz	+6.5			
	F_{RR}	D/A Reference input signal 1015 Hz 0 dBm0	0 to 3000 Hz	–0.15		+0.15	
			3200 Hz	–0.15		+0.65	
			3400 Hz	0		+0.8	
			3780 Hz	+6.5			
Gain tracking (tone method)	GT_X	A/D Reference input signal –10 dBm0 f = 700 to 1100 Hz	+3 to –40 dBm0	–0.2		+0.2	dB
			–50 dBm0	–0.5		+0.5	
			–55 dBm0	–1.0		+1.0	
	GT_R	D/A Reference input signal –10 dBm0 f = 700 to 1100 Hz	+3 to –40 dBm0	–0.2		+0.2	
			–50 dBm0	–0.5		+0.5	
			–55 dBm0	–1.0		+1.0	
Transmit/receive channel overall power distortion ratio (tone method)	SD_X	A/D Input signal f = 700 to 1100 Hz	+3 to –30 dBm0	36			dB
			–40 dBm0	30			
			–45 dBm0	25			
	SD_R	D/A Input signal f = 700 to 1100 Hz	+3 to –30 dBm0	36			
			–40 dBm0	30			
			–45 dBm0	25			
Absolute delay characteristic	D_A	A/A Input signal = 0 dBm0				540	μs
Absolute delay distortion frequency characteristics	D_O	A/A	500 Hz			1400	μs
			600 Hz			700	
			1000 to 2600 Hz			200	
			2800 Hz			1400	
Idle channel noise	ICN_{ADA}	A/D A-law Psophometric weighted				–72	dBm0p
	ICN_{DAA}	D/A A-law Psophometric weighted				–80	
	$ICN_{AD\mu}$	A/D μ-law C-message weighted				18	dBrnc0
	$ICN_{DA\mu}$	D/A μ-law C-message weighted				10	

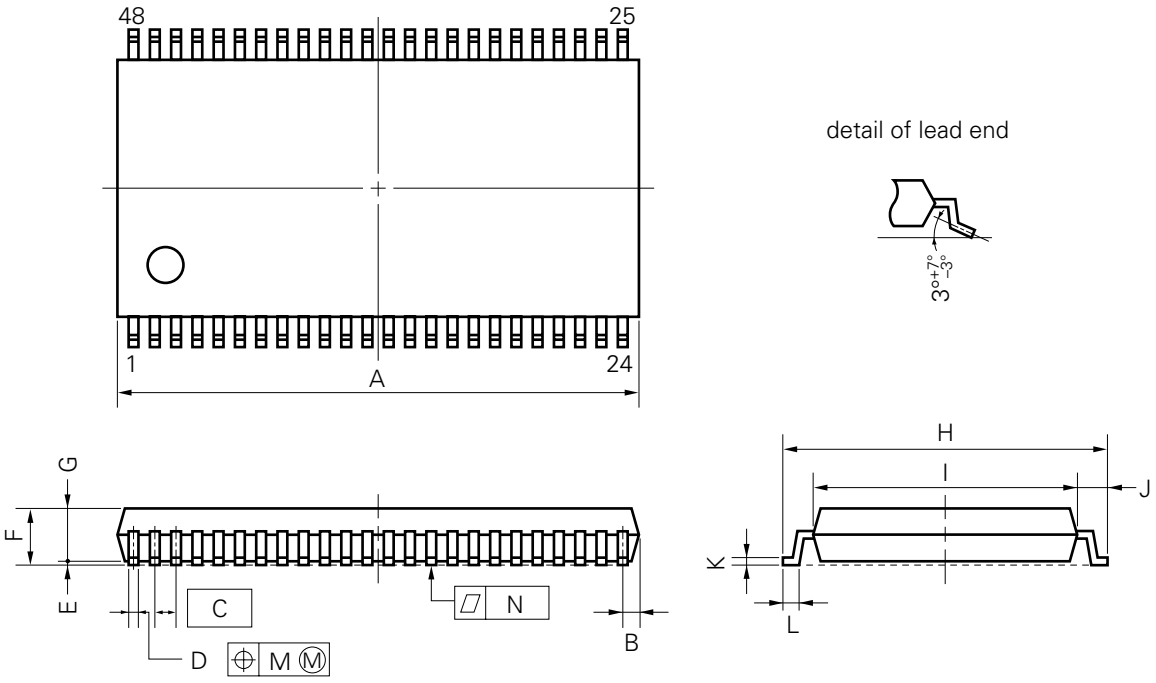
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Cross talk between channels	CT	A/A Input signal = 0 dBm0			–70	dB
Power supply rejection ratio	PSRR	$AV_{DD}1$, $AV_{DD}2$, $AV_{DD}3$, $AV_{DD}4$, DV_{DD} = 5 V ± 100 mV_{P-P}			–25	dB
Coder offset		A/D Input signal 0 V	–5		+5	–
Mutual modulation (2 tones)	IMD	A/D Input signal: f1, f2; 300 to 3400 Hz, –4 to –21 dBm0 Measuring signal: 2 × f1 – f2 level (2 × f1 – f2) vs level (f1, f2)	44.0			dB
		D/A Input signal: f1, f2; 300 to 3400Hz, –4 to –21 dBm0 Measuring signal: 2 × f1 – f2 level (2 × f1 – f2) vs level (f1, f2)	44.0			dB
Discrimination		A/D Input signal: f; 4396 to 7796 Hz 0 dBm0 Measuring signal: 8000 – fHz			–27	dB
Out-of-band spurious		D/A Input signal: f; 204 to 3604 Hz 0 dBm0 Measuring signal: 8000 – fHz			–27	dB
In-band spurious		A/D Input signal: f; 700 to 1100 Hz 0 dBm0 Measuring signal: Any frequency			–45	dB
		D/A Input signal: f; 700 to 1100 Hz 0 dBm0 Measuring signal: Any frequency			–45	dB
Single frequency noise	N_{SF}	D/A Gain setting = 0 dB Measuring signal: f = up to 256 kHz			–54	dBm0
Transmit gain setting	ΔDGS_X	A/D difference from reference setting value	–0.15		+0.15	dB
Receive gain setting	ΔDGS_R	D/A difference from reference setting value	–0.15		+0.15	

5. APPLICATION CIRCUIT EXAMPLE



6. PACKAGE DRAWINGS

48 PIN PLASTIC SHRINK SOP (375 mil)



P48GT-65-375B-1

NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.21 MAX.	0.639 MAX.
B	0.63 MAX.	0.025 MAX.
C	0.65 (T.P.)	0.026 (T.P.)
D	0.30±0.10	$0.012^{+0.004}_{-0.005}$
E	0.125±0.075	0.005±0.003
F	2.0 MAX.	0.079 MAX.
G	1.7±0.1	0.067±0.004
H	10.0±0.3	$0.394^{+0.012}_{-0.013}$
I	8.0±0.2	0.315±0.008
J	1.0±0.2	$0.039^{+0.009}_{-0.008}$
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	0.10	0.004
N	0.10	0.004

7. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended below.

For details of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

SURFACE MOUNT TYPE

μPD9611GT: 48-pin shrink SOP (375 mil)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C Duration: 30 sec. max. (210 °C or above) Number of times: 2 max. Time limit: 3 days[Note] (thereafter, 10-hour prebaking at 125 °C required.) **<Cautions>** (1) Wait for the device temperature to return to normal after the first reflow before starting the second reflow. (2) Do not perform flux cleaning with water after the first reflow.	IR-35-103-2
Pin heating	Pin temperature: 300 °C max. Duration: 3 sec. max. (per side of device)	—

Note For the storage period after unpacking from the dry-pack, storage conditions are max. 25 °C, 65 % RH.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

M4 96.5