Virtex-6 FPGA Data Sheet: DC and Switching Characteristics

DS152 (v2.10) October18, 2010 **Advance Product Specification**

Virtex-6 FPGA Electrical Characteristics

Virtex®-6 FPGAs are available in -3, -2, -1, and -1L speed grades, with -3 having the highest performance. Virtex-6 FPGA DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This Virtex-6 FPGA data sheet, part of an overall set of documentation on the Virtex-6 family of FPGAs, is available on the Xilinx website.

All specifications are subject to change without notice.

Virtex-6 FPGA DC Characteristics

Table 1: **Absolute Maximum Ratings** (1)

Symbol	Description		Units
V_{CCINT}	Internal supply voltage relative to GND	–0.5 to 1.1	V
	For -1L devices: Internal supply voltage relative to GND	–0.5 to 1.0	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 3.0	V
V_{CCO}	Output drivers supply voltage relative to GND	–0.5 to 3.0	V
V_{BATT}	Key memory battery backup supply	–0.5 to 3.0	V
V_{FS}	External voltage supply for eFUSE programming(2)	–0.5 to 3.0	V
V_{REF}	Input reference voltage	–0.5 to 3.0	V
V_{IN}(3)	2.5V or below I/O input voltage relative to GND(4) (user and dedicated I/Os)	–0.5 to V_{CCO} + 0.5	V
V_{TS}	Voltage applied to 3-state 2.5V or below output(4) (user and dedicated I/Os)	–0.5 to V_{CCO} + 0.5	V
T_{STG}	Storage temperature (ambient)	–65 to 150	°C
T_{SOL}	Maximum soldering temperature(5)	+220	°C
T_j	Maximum junction temperature(5)	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. When not programming eFUSE, connect V_{FS} to GND.
3. 2.5V I/O absolute maximum limit applied to DC and AC signals.
4. For I/O operation, refer to the *Virtex-6 FPGA SelectIO Resources User Guide*.
5. For soldering guidelines and thermal considerations, see *Virtex-6 FPGA Packaging and Pinout Specification*.

Table 2: **Recommended Operating Conditions**

Symbol	Description	Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND, T_j = 0°C to +85°C	0.95	1.05	V
	For -1L commercial temperature range devices: internal supply voltage relative to GND, T_j = 0°C to +85°C	0.87	0.93	V
	For -1L industrial temperature range devices: internal supply voltage relative to GND, T_j = –40°C to +100°C	0.91	0.97	V
V_{CCAUX}	Auxiliary supply voltage relative to GND, T_j = 0°C to +85°C	2.375	2.625	V
V_{CCO}(1)(3)(4)	Supply voltage relative to GND, T_j = 0°C to +85°C	1.14	2.625	V
V_{IN}	2.5V supply voltage relative to GND, T_j = 0°C to +85°C	GND – 0.20	2.625	V
	2.5V and below supply voltage relative to GND, T_j = 0°C to +85°C	GND – 0.20	V_{CCO} + 0.2	V
I_{IN}(6)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	10	mA
V_{BATT}(2)	Battery voltage relative to GND, T_j = 0°C to +85°C	1.0	2.5	V
V_{FS}(7)	External voltage supply for eFUSE programming	2.375	2.625	V

Notes:

1. Configuration data is retained even if V_{CCO} drops to 0V.
2. V_{BATT} is required only when using bitstream encryption. If battery is not used, connect V_{BATT} to either ground or V_{CCAUX}.
3. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, and 2.5V.
4. The configuration supply voltage V_{CC_CONFIG} is also known as V_{CCO_0}.
5. All voltages are relative to ground.
6. A total of 100 mA per bank should not be exceeded.
7. When not programming eFUSE, connect V_{FS} to GND.

Table 3: **DC Characteristics Over Recommended Operating Conditions** (1)(2)

Symbol	Description	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	10	µA
I_L	Input or output leakage current per pin (sample-tested)	–	–	10	µA
C_{IN}(3)	Die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V	20	–	80	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V	8	–	40	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V	5	–	30	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V	1	–	20	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 2.5V	3	–	80	µA
I_{BATT}	Battery supply current	–	–	150	nA
n	Temperature diode ideality factor	–	1.0002	–	n
r	Series resistance	–	5	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Maximum value specified for worst case process at 25°C.
3. This measurement represents the die capacitance at the pad, not including the package.

Important Note

Typical values for quiescent supply current are specified at nominal voltage, 85°C junction temperatures (T_j). Xilinx recommends analyzing static power consumption at T_j = 85°C because the majority of designs operate near the high end of the commercial temperature range. Quiescent supply current is specified by speed grade for Virtex-6 devices. Use the XPOWER™ Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified in Table 4.

Table 4: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed and Temperature Grade					Units
			-3 (C)	-2 (C & I)(1)	-1 (C & I)	-1L (C)	-1L (I)(2)	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC6VLX75T	927	927	927	656	741	mA
		XC6VLX130T	1563	1563	1563	1102	1245	mA
		XC6VLX195T	2059	2059	2059	1441	1628	mA
		XC6VLX240T	2478	2478	2478	1733	1957	mA
		XC6VLX365T	3001	3001	3001	2092	2363	mA
		XC6VLX550T	N/A	4515	4515	3147	3555	mA
		XC6VLX760	N/A	5094	5094	3471	3921	mA
		XC6VSX315T	3476	3476	3476	2409	2721	mA
		XC6VSX475T	N/A	5227	5227	3622	4091	mA
		XC6VHX250T	2906	2906	2906	N/A	N/A	mA
		XC6VHX255T				N/A	N/A	mA
		XC6VHX380T				N/A	N/A	mA
		XC6VHX565T	N/A			N/A	N/A	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC6VLX75T	1	1	1	1	1	mA
		XC6VLX130T	1	1	1	1	1	mA
		XC6VLX195T	1	1	1	1	1	mA
		XC6VLX240T	2	2	2	2	2	mA
		XC6VLX365T	2	2	2	2	2	mA
		XC6VLX550T	N/A	3	3	3	3	mA
		XC6VLX760	N/A	3	3	3	3	mA
		XC6VSX315T	2	2	2	2	2	mA
		XC6VSX475T	N/A	2	2	2	2	mA
		XC6VHX250T	1	1	1	N/A	N/A	mA
		XC6VHX255T				N/A	N/A	mA
		XC6VHX380T				N/A	N/A	mA
		XC6VHX565T	N/A			N/A	N/A	mA

Table 4: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed and Temperature Grade					Units
			-3 (C)	-2 (C & I)[1]	-1 (C & I)	-1L (C)	-1L (I)[2]	
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC6VLX75T	45	45	45	45	45	mA
		XC6VLX130T	75	75	75	75	75	mA
		XC6VLX195T	113	113	113	113	113	mA
		XC6VLX240T	135	135	135	135	135	mA
		XC6VLX365T	191	191	191	191	191	mA
		XC6VLX550T	N/A	286	286	286	286	mA
		XC6VLX760	N/A	387	387	387	387	mA
		XC6VSX315T	186	186	186	186	186	mA
		XC6VSX475T	N/A	279	279	279	279	mA
		XC6VHX250T	152	152	152	N/A	N/A	mA
		XC6VHX255T				N/A	N/A	mA
		XC6VHX380T				N/A	N/A	mA
		XC6VHX565T	N/A			N/A	N/A	mA

Notes:

1. The XC6VLX550T, XC6VLX760, XC6VSX475T, and XC6VHX565T are not offered in -2I.
2. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j). -1, -2, and -3 industrial (I) grade devices have the same typical values as commercial (C) grade devices at 85°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. -1L industrial grade devices have the values specified in this column.
3. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
4. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

Virtex-6 devices require a power-on sequence of V_{CCINT}, V_{CCAUX}, and V_{CCO}. If the requirement can not be met, then V_{CCAUX} must always be powered prior to V_{CCO}. V_{CCAUX} and V_{CCO} can be powered by the same supply, therefore, both V_{CCAUX} and V_{CCO} are permitted to ramp simultaneously. Similarly, for the power-down sequence, V_{CCO} must be powered down prior to V_{CCAUX} or if power by the same supply, V_{CCAUX} and V_{CCO} power-down simultaneously.

Table 5 shows the minimum current, in addition to I_{CCQ}, that are required by Virtex-6 devices for proper power-on and configuration. If the current minimums shown in Table 4 and Table 5 are met, the device powers on after all three supplies have passed through their power-on reset threshold voltages. The FPGA must be configured after V_{CCINT} is applied.

Once initialized and configured, use the XPOWER tools to estimate current drain on these supplies.

Table 5: **Power-On Current for Virtex-6 Devices**

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	Units
	Typ(1)	Typ(1)	Typ(1)	
XC6VLX75T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 10	I_{CCOQ} + 30 mA per bank	mA
XC6VLX130T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 10	I_{CCOQ} + 30 mA per bank	mA
XC6VLX195T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VLX240T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VLX365T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VLX550T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VLX760	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VSX315T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VSX475T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 50	I_{CCOQ} + 30 mA per bank	mA
XC6VHX250T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VHX255T				mA
XC6VHX380T				mA
XC6VHX565T				mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Use the XPOWER™ Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate maximum power-on currents.

Table 6: **Power Supply Ramp Time**

Symbol	Description	Ramp Time	Units
V_{CCINT}	Internal supply voltage relative to GND	0.20 to 50.0	ms
V_{CCO}	Output drivers supply voltage relative to GND	0.20 to 50.0	ms
V_{CCAUX}	Auxiliary supply voltage relative to GND	0.20 to 50.0	ms

SelectIO™ DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 7: **SelectIO DC Input and Output Levels**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVCMOS25, LVDCI25	–0.3	0.7	1.7	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	Note(3)	Note(3)
LVCMOS18, LVDCI18	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	0.45	V_{CCO} – 0.45	Note(4)	Note(4)
LVCMOS15, LVDCI15	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note(4)	Note(4)
LVCMOS12	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note(5)	Note(5)
HSTL I_12	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	6.3	6.3
HSTL I(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	8	–8
HSTL II(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	16	–16
HSTL III(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	24	–8
DIFF HSTL I(2)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
DIFF HSTL II(2)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
SSTL2 I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2 II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
DIFF SSTL2 I	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	–	–	–	–
DIFF SSTL2 II	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	–	–	–	–
SSTL18 I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.47	V_{TT} + 0.47	6.7	–6.7
SSTL18 II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.60	V_{TT} + 0.60	13.4	–13.4
DIFF SSTL18 I	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–
DIFF SSTL18 II	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–
SSTL15	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	V_{TT} – 0.175	V_{TT} + 0.175	14.3	14.3

Notes:

1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. Supported drive strengths of 2, 4, 6, or 8 mA.
6. For detailed interface specific DC voltage levels, see the *Virtex-6 FPGA SelectIO Resources User Guide*.

HT DC Specifications (HT_25)

Table 8: **HT DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OD}	Differential Output Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	480	600	885	mV
ΔV_{OD}	Change in V_{OD} Magnitude		–15	–	15	mV
V_{OCM}	Output Common Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	440	600	760	mV
ΔV_{OCM}	Change in V_{OCM} Magnitude		–15	–	15	mV
V_{ID}	Input Differential Voltage		200	600	1000	mV
ΔV_{ID}	Change in V_{ID} Magnitude		–15	–	15	mV
V_{ICM}	Input Common Mode Voltage		440	600	780	mV
ΔV_{ICM}	Change in V_{ICM} Magnitude		–15	–	15	mV

LVDS DC Specifications (LVDS_25)

Table 9: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDSEXT_25)

Table 10: **Extended LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.785	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.715	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	350	–	840	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	–	1000	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 11 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-6 FPGA SelectIO Resources User Guide*.

Table 11: **LVPECL DC Specifications**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{OH}	Output High Voltage	V_{CC} – 1.025	1.545	V_{CC} – 0.88	V
V_{OL}	Output Low Voltage	V_{CC} – 1.81	0.795	V_{CC} – 1.62	V
V_{ICM}	Input Common-Mode Voltage	0.6	–	2.2	V
V_{IDIFF}	Differential Input Voltage(1)(2)	0.100	–	1.5	V

Notes:

1. Recommended input maximum voltage not to exceed V_{CCAUX} + 0.2V.
2. Recommended input minimum voltage not to go below –0.5V.

eFUSE Read Endurance

Table 12 lists the maximum number of read cycle operations expected. For more information, see the *Virtex-6 FPGA Configuration User Guide*.

Table 12: **eFUSE Read Endurance**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles

GTX Transceiver Specifications

GTX Transceiver DC Characteristics

Table 13: **Absolute Maximum Ratings for GTX Transceivers(1)**

Symbol	Description	Min	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	–0.5	1.1	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	–0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.32	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.32	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 14: **Recommended Operating Conditions for GTX Transceivers(1)(2)**

Symbol	Description	Speed Grade	PLL Frequency	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	-3, -2(3)	> 2.7 GHz	1.0	1.03	1.06	V
		-3, -2(3)	≤ 2.7 GHz	0.95	1.0	1.06	V
		-1	≤ 2.7 GHz	0.95	1.0	1.06	V
		-1L	≤ 2.7 GHz	0.95	1.0	1.05	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	All	–	1.14	1.2	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	All	–	1.14	1.2	1.26	V

Notes:

1. Each voltage listed requires the filter circuit described in *Virtex-6 FPGA GTX Transceivers User Guide*.
2. Voltages are specified for the temperature range of T_j = –40°C to +100°C.
3. If a GTX Quad contains transceivers operating with a mixture of PLL frequencies above and below 2.7 GHz, the MGTAVCC voltage supply must be in the range of 1.0V to 1.06V.

Table 15: **GTX Transceiver Supply Current (per Lane) (1)(2)**

Symbol	Description	Typ	Max	Units
$I_{MGTAVTT}$	MGTAVTT supply current for one GTX transceiver	55.9	Note 2	mA
$I_{MGTAVCC}$	MGTAVCC supply current for one GTX transceiver	56.1		mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	100.0 ± 1% tolerance		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 3.125 Gb/s line rate.
2. Values for currents of other transceiver configurations and conditions can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 16: **GTX Transceiver Quiescent Supply Current (per Lane) (1)(2)(3)**

Symbol	Description	Typ(4)	Max	Units
$I_{MGTAVTTQ}$	Quiescent MGTAVTT supply current for one GTX transceiver	0.9	Note 2	mA
$I_{MGTAVCCQ}$	Quiescent MGTAVCC supply current for one GTX transceiver	3.5		mA

Notes:

1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
3. GTX transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTX transceivers.
4. Typical values are specified at nominal voltage, 25°C.

GTX Transceiver DC Input and Output Levels

Table 17 summarizes the DC output specifications of the GTX transceivers in Virtex-6 FPGAs. Consult the *Virtex-6 FPGA GTX Transceivers User Guide* for further details.

Table 17: **GTX Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled ≤ 4.25 Gb/s	125	–	2000	mV
		External AC coupled > 4.25 Gb/s	175	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled MGTAVTT = 1.2V	–400	–	MGTAVTT	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTAVTT = 1.2V	–	2/3 MGTAVTT	–	mV
DV_{PPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to maximum setting	–	–	1000	mV
$V_{CMOUTDC}$	DC common mode output voltage.	Equation based	MGTAVTT – DV_{PPOUT}/4			mV
R_{IN}	Differential input resistance		80	100	130	Ω
R_{OUT}	Differential output resistance		80	100	120	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	8	ps
C_{EXT}	Recommended external AC coupling capacitor(2)		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in the *Virtex-6 FPGA GTX Transceivers User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

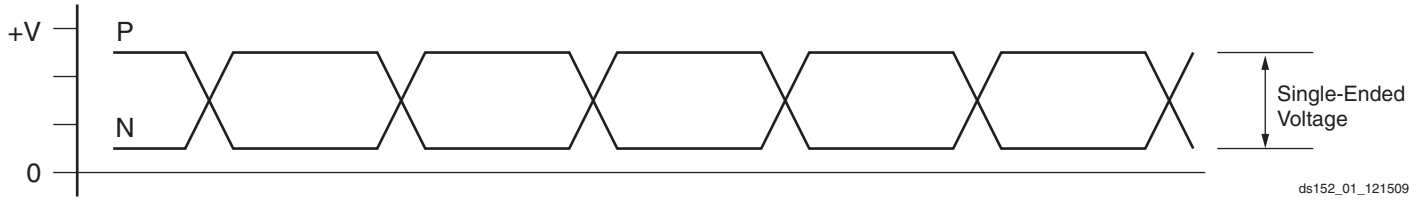

Figure 1: **Single-Ended Peak-to-Peak Voltage**

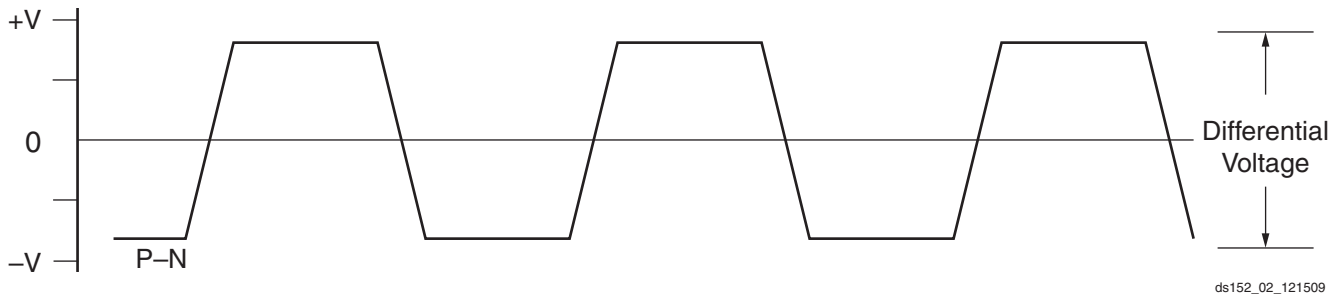

Figure 2: **Differential Peak-to-Peak Voltage**

Table 18 summarizes the DC specifications of the clock input of the GTX transceiver. Consult the *Virtex-6 FPGA GTX Transceivers User Guide* for further details.

Table 18: **GTX Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage		210	800	2000	mV
R_{IN}	Differential input resistance		90	100	130	Ω
C_{EXT}	Required external AC coupling capacitor		–	100	–	nF

GTX Transceiver Switching Characteristics

Consult *Virtex-6 FPGA GTX Transceivers User Guide* for further information.

Table 19: **GTX Transceiver Performance**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F_{GTXMAX}	Maximum GTX transceiver data rate	6.6	6.6	5.0	5.0	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	3.3(1)	3.3(1)	2.7	2.7	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	1.2	1.2	1.2	1.2	GHz

Notes:

1. See Table 14 for MGTAVCC requirements when PLL frequency is greater than 2.7 GHz.

Table 20: **GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$F_{GTXDRPCLK}$	GTXDRPCLK maximum frequency	150	150	125	100	MHz

Table 21: **GTX Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		62.5	–	650	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	–	1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	–	–	200	µs

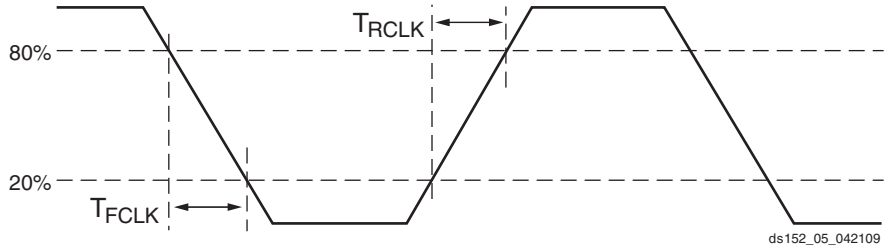

Figure 3: **Reference Clock Timing Parameters**

Table 22: **GTX Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Conditions	Speed Grade				Units
			-3	-2	-1	-1L	
F_{TXOUT}	TXOUTCLK maximum frequency	Internal 20-bit data path	330	330	250	250	MHz
		Internal 16-bit data path	412.5	412.5	312.5	250	MHz
F_{RXREC}	RXRECCLK maximum frequency	Internal 20-bit data path	330	330	250	250	MHz
		Internal 16-bit data path	412.5	412.5	312.5	250	MHz
T_{RX}	RXUSRCLK maximum frequency		412.5(2)	412.5(2)	312.5	250	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	376	376	312.5	250	MHz
		2 byte interface	406.25	406.25	312.5	250	MHz
		4 byte interface	206.25	206.25	156.25	125	MHz
T_{TX}	TXUSRCLK maximum frequency		412.5(3)	412.5(3)	312.5	250	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	376	376	312.5	250	MHz
		2 byte interface	406.25	406.25	312.5	250	MHz
		4 byte interface	206.25	206.25	156.25	125	MHz

Notes:

1. Clocking must be implemented as described in the *Virtex-6 FPGA GTX Transceivers User Guide*.
2. 406.25 MHz when the RX elastic buffer is bypassed.
3. 406.25 MHz when the TX buffer is bypassed.

Table 23: **GTX Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTXTX}	Serial data rate range		0.480	–	F_{GTXMAX}	Gb/s
T_{RTX}	TX Rise time	20%–80%	–	120	–	ps
T_{FTX}	TX Fall time	80%–20%	–	120	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	350	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	15	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	75	ns
$TJ_{6.5}$	Total Jitter(2)(3)	6.5 Gb/s	–	–	0.33	UI
$DJ_{6.5}$	Deterministic Jitter(2)(3)		–	–	0.17	UI
$TJ_{5.0}$	Total Jitter(2)(3)	5.0 Gb/s	–	–	0.33	UI
$DJ_{5.0}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{4.25}$	Total Jitter(2)(3)	4.25 Gb/s	–	–	0.33	UI
$DJ_{4.25}$	Deterministic Jitter(2)(3)		–	–	0.14	UI
$TJ_{3.75}$	Total Jitter(2)(3)	3.75 Gb/s	–	–	0.34	UI
$DJ_{3.75}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$TJ_{3.125}$	Total Jitter(2)(3)	3.125 Gb/s	–	–	0.2	UI
$DJ_{3.125}$	Deterministic Jitter(2)(3)		–	–	0.1	UI
$TJ_{3.125L}$	Total Jitter(2)(3)	3.125 Gb/s(4)	–	–	0.35	UI
$DJ_{3.125L}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$TJ_{2.5}$	Total Jitter(2)(3)	2.5 Gb/s(5)	–	–	0.20	UI
$DJ_{2.5}$	Deterministic Jitter(2)(3)		–	–	0.08	UI
$TJ_{1.25}$	Total Jitter(2)(3)	1.25 Gb/s(6)	–	–	0.15	UI
$DJ_{1.25}$	Deterministic Jitter(2)(3)		–	–	0.06	UI
TJ_{600}	Total Jitter(2)(3)	600 Mb/s	–	–	0.1	UI
DJ_{600}	Deterministic Jitter(2)(3)		–	–	0.03	UI
TJ_{480}	Total Jitter(2)(3)	480 Mb/s	–	–	0.1	UI
DJ_{480}	Deterministic Jitter(2)(3)		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
2. Using PLL_DIVSEL_FB = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. All jitter values are based on a bit-error ratio of $1e^{-12}$.
4. PLL frequency at 1.5625 GHz and OUTDIV = 1.
5. PLL frequency at 2.5 GHz and OUTDIV = 2.
6. PLL frequency at 2.5 GHz and OUTDIV = 4.

Table 24: **GTX Transceiver Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTXRX}	Serial data rate	RX oversampler not enabled	0.600	–	F_{GTXMAX}	Gb/s
		RX oversampler enabled	0.480	–	0.600	Gb/s
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data		–	75	–	ns
$RX_{OOBVDPP}$	OOB detect threshold peak-to-peak		60	–	150	mV
RX_{SST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz	–5000	–	0	ppm
RX_{RL}	Run length (CID)	Internal AC capacitor bypassed	–	–	512	UI
RX_{PPMTOL}	Data/REFCLK PPM offset tolerance	CDR 2nd-order loop disabled	–200	–	200	ppm
		CDR 2nd-order loop enabled	–2000	–	2000	ppm
SJ Jitter Tolerance(2)						
$JT\_SJ_{6.5}$	Sinusoidal Jitter(3)	6.5 Gb/s	0.44	–	–	UI
$JT\_SJ_{5.0}$	Sinusoidal Jitter(3)	5.0 Gb/s	0.44	–	–	UI
$JT\_SJ_{4.25}$	Sinusoidal Jitter(3)	4.25 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.75}$	Sinusoidal Jitter(3)	3.75 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.125}$	Sinusoidal Jitter(3)	3.125 Gb/s	0.45	–	–	UI
$JT\_SJ_{3.125L}$	Sinusoidal Jitter(3)	3.125 Gb/s(4)	0.45	–	–	UI
$JT\_SJ_{2.5}$	Sinusoidal Jitter(3)	2.5 Gb/s(5)	0.5	–	–	UI
$JT\_SJ_{1.25}$	Sinusoidal Jitter(3)	1.25 Gb/s(6)	0.5	–	–	UI
JT_SJ_{600}	Sinusoidal Jitter(3)	600 Mb/s	0.4	–	–	UI
JT_SJ_{480}	Sinusoidal Jitter(3)	480 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$JT\_TJSE_{3.125}$	Total Jitter with Stressed Eye(7)	3.125 Gb/s	0.70	–	–	UI
		5.0 Gb/s	0.70	–	–	UI
$JT\_SJSE_{3.125}$	Sinusoidal Jitter with Stressed Eye(7)	3.125 Gb/s	0.1	–	–	UI
		5.0 Gb/s	0.1	–	–	UI

Notes:

1. Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. PLL frequency at 1.5625 GHz and OUTDIV = 1.
5. PLL frequency at 2.5 GHz and OUTDIV = 2.
6. PLL frequency at 2.5 GHz and OUTDIV = 4.
7. Composite jitter with RX equalizer enabled. DFE disabled.

GTH Transceiver Specifications

GTH Transceiver DC Characteristics

Table 25: **Absolute Maximum Ratings for GTH Transceivers(1)**

Symbol	Description	Min	Max	Units
MGTHAVCC	Analog supply voltage for the GTH transmitter, receiver, and common analog circuits	–0.5		V
MGTHAVCCRX	Analog supply voltage for the GTH receiver circuits and common analog circuits	–0.5		V
MGTAVTT	Analog supply voltage for the GTH transmitter termination circuits	–0.5		V
MGTHAVCCPLL	Analog supply voltage for the GTH receiver and PLL circuits	–0.5		V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5		V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5		V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 26: **Recommended Operating Conditions for GTH Transceivers (1)(2)**

Symbol	Description	Min	Typ	Max	Units
MGTHAVCC	Analog supply voltage for the GTH transmitter, receiver, and common analog circuits	1.075	1.1	1.125	V
MGTHAVCCRX	Analog supply voltage for the GTH receiver circuits and common analog circuits	1.075	1.1	1.125	V
MGTHAVTT	Analog supply voltage for the GTH transmitter termination circuits	1.140	1.2	1.26	V
MGTHAVCCPLL	Analog supply voltage for the GTH receiver and PLL circuit	1.710	1.8	1.89	V

Notes:

1. Each voltage listed requires the filter circuit described in *Virtex-6 FPGA GTH Transceivers User Guide*.
2. Voltages are specified for the temperature range of T_j = –40°C to +100°C.

Table 27: **GTH Transceiver Power Supply Sequencing (1)(2)**

Symbol	Description	Min	Max	Units
$T_{HAVCC2HAVCCRX}$	Maximum time between powering MGTHAVCC to when MGTHAVCCRX must be powered.	0	200	µs
$T_{HAVCCRX2HAVCCPLL}$	Minimum time between powering MGTHAVCCRX to when MGTHAVCCPLL can be powered.	10	–	µs
$T_{HAVCCRX2HAVTT}$	Minimum time between powering MGTHAVCCRX to when MGTHAVTT can be powered.	10	–	µs

Notes:

1. MGTHAVCCRX must be powered simultaneously or within $T_{HAVCC2HAVCCRX}$ of MGTHAVCC, but it must not precede MGTHAVCC.
2. MGTHAVCC and MGTHAVCCRX must be powered before MGTHAVCCPLL and MGTHAVTT. This minimum time is defined by $T_{HAVCCRX2HAVCCPLL}$ and $T_{HAVCCRX2HAVTT}$.

Figure 4 shows the timing parameters in Table 27.

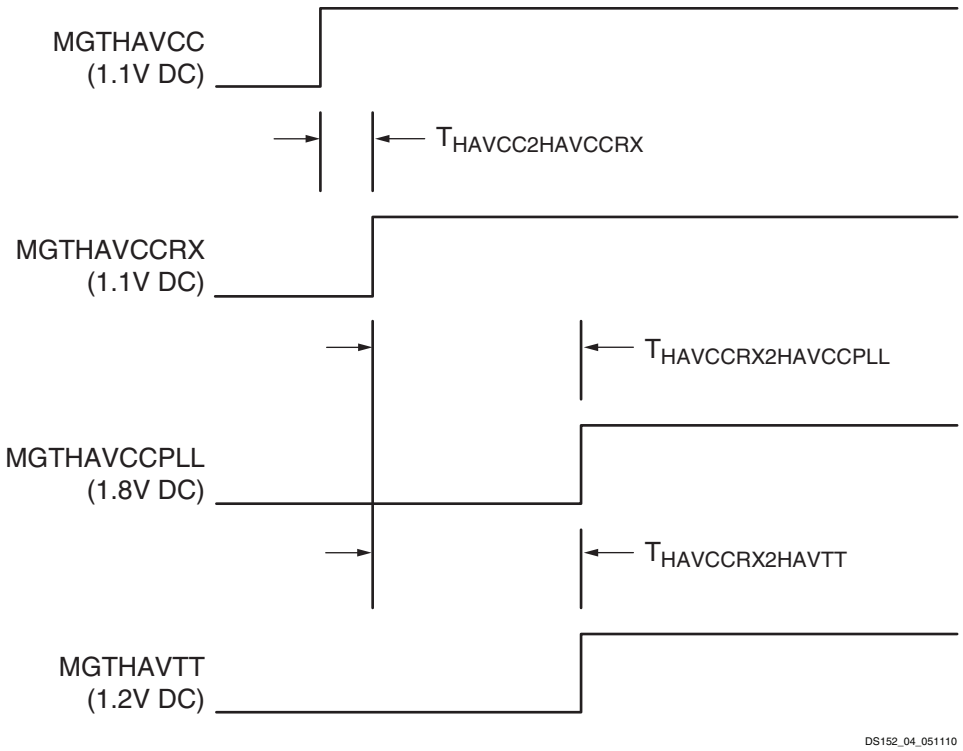

Figure 4: **GTH Transceiver Power Supply Power-On Sequencing**

Table 28: **GTH Transceiver Supply Current (1)(2)**

Symbol	Description	Min	Typ	Max	Units
$I_{MGTHAVCC}$	MGTHAVCC supply current for one GTH Quad (4 lanes)				mA
$I_{MGTHAVCCRX}$	MGTHAVCCRX supply current for a GTH Quad (4 lanes)				mA
$I_{MGTHAVTT}$	MGTHAVTT supply current for one GTH Quad (4 lanes)				mA
$I_{MGTHAVCCPLL}$	MGTHAVCCPLL supply current for one GTH Quad (4 lanes)				mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	1000.0 ± 1% tolerance			Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 10.3125 Gb/s line rate.
2. Values for currents other than the values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 29: **GTH Transceiver Quiescent Supply Current(1)(2)(3)**

Symbol	Description	Typ(4)	Max	Units
$I_{MGTHAVCCQ}$	Quiescent MGTHAVCC Supply Current for one GTH Quad (4 lanes)			mA
$I_{MGTHAVCCRXQ}$	Quiescent MGTHAVCCRX Supply Current for one GTH Quad (4 lanes)			mA
$I_{MGTHAVTTQ}$	Quiescent MGTHAVTT Supply Current for one GTH Quad (4 lanes)			mA
$I_{MGTHAVCCPLLQ}$	Quiescent MGTHAVCCPLL Supply Current for one GTH Quad (4 lanes)			mA

Notes:

1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
3. GTH transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTH transceivers.
4. Typical values are specified at nominal voltage, 25°C.

GTH Transceiver DC Input and Output Levels

Table 30 summarizes the DC output specifications of the GTH transceivers in Virtex-6 FPGAs. Consult the *Virtex-6 FPGA GTH Transceivers User Guide* for further details.

Table 30: **GTH Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
D_{VPPIN}	Differential peak-to-peak input voltage	External AC coupled				mV
D_{VPPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to maximum setting				mV
R_{IN}	Differential input resistance			100		Ω
R_{OUT}	Differential output resistance			100		Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew					ps
C_{EXT}	Recommended external AC coupling capacitor(2)			100		nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in the *Virtex-6 FPGA GTH Transceivers User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

Table 31 summarizes the DC specifications of the clock input of the GTH transceiver. Consult the *Virtex-6 FPGA GTH Transceivers User Guide* for further details.

Table 31: **GTH Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	≤ 600 MHz	500		1600	mV
		> 600 MHz	600		1600	mV
R_{IN}	Differential input resistance			100		Ω
C_{EXT}	Required external AC coupling capacitor			100		nF

GTH Transceiver Switching Characteristics

Consult *Virtex-6 FPGA GTH Transceivers User Guide* for further information.

Table 32: **GTH Transceiver Maximum Data Rate and PLL Frequency Range**

Symbol	Description	Conditions	Speed Grade			Units
			-3	-2	-1	
F_{GTHMAX}	Maximum GTH transceiver data rate	PLL Output Divider = 1	11.182	11.182	10.32	Gb/s
		PLL Output Divider = 4	2.795	2.795	2.58	Gb/s
F_{GTHMIN}	Minimum GTH transceiver data rate(1)	PLL Output Divider = 1	9.92	9.92	9.92	Gb/s
		PLL Output Divider = 4	2.48	2.48	2.48	Gb/s
$F_{GPLLMAX}$	Maximum GTH PLL frequency		5.591	5.591	5.16	GHz
$F_{GPLLMIN}$	Minimum GTH PLL frequency		4.96	4.96	4.96	GHz

Notes:

1. Lower data rates can be achieved using FPGA logic based oversampling designs.

Table 33: **GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{GTHDRPCLK}$	GTHDRPCLK maximum frequency	70	70	60	MHz

Table 34: **GTH Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range	-1 speed grade	150		623	MHz
		-2 and -3 speed grades	150		670	MHz
T_{RCLK}	Reference clock rise time	20% – 80%		200		ps
T_{FCLK}	Reference clock fall time	80% – 20%		200		ps
T_{DCREF}	Reference clock duty cycle	CLK	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock				ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock				µs

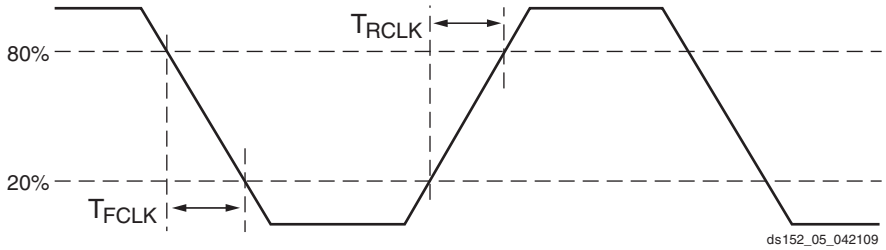

Figure 5: **Reference Clock Timing Parameters**

Table 35: **GTH Transceiver User Clock Switching Characteristics (1)**

Symbol	Description	Conditions	Speed Grade			Units
			-3	-2	-1	
F_{TXOUT}	TXUSERCLKOUT maximum frequency		350	350	323	MHz
F_{RXOUT}	RXUSERCLKOUT maximum frequency		350	350	323	MHz
F_{TXIN}	TXUSERCLKIN maximum frequency	16-bit data path	350	350	323	MHz
		20-bit data path	280	280	258	MHz
		32-bit data path	350	350	323	MHz
		40-bit data path	280	280	258	MHz
		64-bit data path	175	175	162	MHz
		80-bit data path	140	140	129	MHz
		64B/66B-bit data path	170	170	157	MHz
F_{RXIN}	RXUSERCLKIN maximum frequency	16-bit data path	350	350	323	MHz
		20-bit data path	280	280	258	MHz
		32-bit data path	350	350	323	MHz
		40-bit data path	280	280	258	MHz
		64-bit data path	175	175	162	MHz
		80-bit data path	140	140	129	MHz
		64B/66B-bit data path	170	170	157	MHz

Notes:

1. Clocking must be implemented as described in the *Virtex-6 FPGA GTH Transceivers User Guide*.

Table 36: **GTH Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
T_{RTX}	TX Rise time	20%–80%				ps
T_{FTX}	TX Fall time	80%–20%				ps
T_{LLSKEW}	TX lane-to-lane skew	within one GTH Quad				ps
		across multiple GTH Quads				ps
Transmitter Output Jitter(1)(2)						
$TJ_{11.18}$	Total Jitter	11.181 Gb/s				UI
$DJ_{11.18}$	Deterministic Jitter					UI
$TJ_{10.3125}$	Total Jitter	10.3125 Gb/s				UI
$DJ_{10.3125}$	Deterministic Jitter					UI
$TJ_{9.953}$	Total Jitter	9.953 Gb/s				UI
$DJ_{9.953}$	Deterministic Jitter					UI
$TJ_{2.667}$	Total Jitter	2.667 Gb/s				UI
$DJ_{2.667}$	Deterministic Jitter					UI
$TJ_{2.488}$	Total Jitter	2.488 Gb/s				UI
$DJ_{2.488}$	Deterministic Jitter					UI

Notes:

1. These values are NOT intended for protocol specific compliance determinations.
2. All jitter values are based on a bit-error ratio of $1e^{-12}$.

Table 37: **GTH Transceiver Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
R_{XRL}	Run length (CID)					UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance		–200		200	ppm
SJ Jitter Tolerance(1)(2)(3)						
$JT\_SJ_{11.18}$	Sinusoidal Jitter	11.18 Gb/s				UI
$JT\_SJ_{10.32}$	Sinusoidal Jitter	10.32 Gb/s				UI
$JT\_SJ_{9.95}$	Sinusoidal Jitter	9.95 Gb/s				UI
$JT\_SJ_{2.667}$	Sinusoidal Jitter	2.667 Gb/s				UI
$JT\_SJ_{2.48}$	Sinusoidal Jitter	2.48 Gb/s				UI

Notes:

1. These values are NOT intended for protocol specific compliance determinations.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.

Ethernet MAC Switching Characteristics

Consult *Virtex-6 FPGA Embedded Tri-mode Ethernet MAC User Guide* for further information.

Table 38: **Maximum Ethernet MAC Performance**

Symbol	Description	Conditions	Speed Grade				Units
			-3	-2	-1	-1L	
$F_{TEMACCLIENT}$	Client interface maximum frequency	10 Mb/s – 8-bit width	2.5(1)	2.5(1)	2.5(1)	2.5(1)	MHz
		100 Mb/s – 8-bit width	25(2)	25(2)	25(2)	25(2)	MHz
		1000 Mb/s – 8-bit width	125	125	125	125	MHz
		1000 Mb/s – 16-bit width	62.5	62.5	62.5	62.5	MHz
		2000 Mb/s – 16-bit width	125	125	125	N/A	MHz
		2500 Mb/s – 16-bit width	156.25	156.25	156.25	N/A	MHz
$F_{TEMACPHY}$	Physical interface maximum frequency	10 Mb/s – 4-bit width	2.5	2.5	2.5	2.5	MHz
		100 Mb/s – 4-bit width	25	25	25	25	MHz
		1000 Mb/s – 8-bit width	125	125	125	125	MHz
		2000 Mb/s – 8-bit width	250	250	250	N/A	MHz
		2500 Mb/s – 8-bit width	312.5	312.5	312.5	N/A	MHz

Notes:

1. When not using clock enable, the F_{MAX} is lowered to 1.25 MHz.
2. When not using clock enable, the F_{MAX} is lowered to 12.5 MHz.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
http://www.xilinx.com/technology/protocols/pciexpress.htm

Table 39: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$F_{PIPECLK}$	Pipe clock maximum frequency	250	250	250	250	MHz
$F_{USERCLK}$	User clock maximum frequency	500	500	250	250	MHz
F_{DRPCLK}	DRP clock maximum frequency	250	250	250	250	MHz

System Monitor Analog-to-Digital Converter Specification

Table 40: **Analog-to-Digital Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
AV_{DD} = 2.5V ± 5%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 5.2 MHz, T_j = –40°C to 100°C, Typical values at T_j=+35°C						
DC Accuracy: All external input channels. Both unipolar and bipolar modes.						
Resolution			10	–	–	Bits
Integral Nonlinearity	INL		–	–	±1	LSBs
Differential Nonlinearity	DNL	No missing codes (T_{MIN} to T_{MAX}) Guaranteed Monotonic	–	–	±0.9	LSBs
Unipolar Offset Error (1)		Uncalibrated	–	±2	±30	LSBs
Bipolar Offset Error (1)		Uncalibrated measured in bipolar mode	–	±2	±30	LSBs
Gain Error		Uncalibrated - External Reference	–	±0.2	±2	%
		Uncalibrated - Internal Reference	–	±2	–	%
Bipolar Gain Error (1)		Uncalibrated - External Reference	–	±0.2	±2	%
		Uncalibrated - Internal Reference	–	±2	–	%
Total Unadjusted Error (Uncalibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	–	±10	–	LSBs
		Deviation from ideal transfer function. Internal reference	–	±20	–	LSBs
Total Unadjusted Error (Calibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	–	±1	±2	LSBs
Calibrated Gain Temperature Coefficient		Variation of FS code with temperature	–	±0.01	–	LSB/°C
DC Common-Mode Reject	$CMRR_{DC}$	$V_N = V_{CM}$ = 0.5V ± 0.5V, $V_P – V_N$ = 100mV	–	70	–	dB
Conversion Rate(2)						
Conversion Time - Continuous	t_{CONV}	Number of CLK cycles	26	–	32	
Conversion Time - Event	t_{CONV}	Number of CLK cycles	–	–	21	
T/H Acquisition Time	t_{ACQ}	Number of CLK cycles	4	–	–	
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	80	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	5.2	MHz
CLK Duty cycle			40	–	60	%

Table 40: **Analog-to-Digital Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Analog Inputs[3]						
Dedicated Analog Inputs Input Voltage Range V_P - V_N		Unipolar Operation	0	–	1	Volts
		Bipolar Operation	–0.5	–	+0.5	
		Unipolar Common Mode Range (FS input)	0	–	+0.5	
		Bipolar Common Mode Range (FS input)	+0.5	–	+0.6	
		Bandwidth	–	20	–	MHz
Auxiliary Analog Inputs Input Voltage Range $V_{AUXP[0]}$ /$V_{AUXN[0]}$ to $V_{AUXP[15]}$ /$V_{AUXN[15]}$ T_j = –40°C to 100°C		Unipolar Operation	0	–	1	Volts
		Bipolar Operation	–0.5	–	+0.5	
		Unipolar Common Mode Range (FS input)	0	–	+0.5	
		Bipolar Common Mode Range (FS input)	+0.5	–	+0.6	
		Bandwidth	–	10	–	kHz
Input Leakage Current		A/D not converting, ADCCLK stopped	–	±1.0	–	µA
Input Capacitance			–	10	–	pF
On-chip Supply Monitor Error		V_{CCINT} and V_{CCAUX} with calibration enabled. External 1.25V reference T_j = –40°C to 125°C.	–	–	±1.0	% Reading
		V_{CCINT} and V_{CCAUX} with calibration enabled. Internal reference T_j = –40°C to 100°C.	–	±2	–	% Reading
On-chip Temperature Monitor Error		T_j = –40°C to +125°C with calibration enabled. External 1.25V reference.	–	–	±4	°C
		T_j = –40°C to +100°C with calibration enabled. Internal reference.	–	±5	–	°C
External Reference Inputs[4]						
Positive Reference Input Voltage Range	V_{REFP}	Measured Relative to V_{REFN}	1.20	1.25	1.30	Volts
Negative Reference Input Voltage Range	V_{REFN}	Measured Relative to AGND	–50	0	100	mV
Input current	I_{REF}	ADCCLK = 5.2 MHz	–	–	100	µA
Power Requirements						
Analog Power Supply	AV_{DD}	Measured Relative to AV_{SS}	2.375	2.5	2.625	Volts
Analog Supply Current	AI_{DD}	ADCCLK = 5.2 MHz	–	–	12	mA

Notes:

1. Offset errors are removed by enabling the System Monitor automatic gain calibration feature.
2. See "System Monitor Timing" in the *Virtex-6 FPGA System Monitor User Guide*
3. See "Analog Inputs" in the *Virtex-6 FPGA System Monitor User Guide* for a detailed description.
4. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result is a deviation from the ideal transfer function.This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-6 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the Switching Characteristics, page 24.

Table 41: **Interface Performances**

Description	Speed Grade			
	-3	-2	-1	-1L
Networking Applications				
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	710 Mb/s	710 Mb/s	650 Mb/s	585 Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 10)	1.4 Gb/s	1.3 Gb/s	1.25 Gb/s	1.1 Gb/s
SDR LVDS receiver (SFI-4.1)(1)	710 Mb/s	710 Mb/s	650 Mb/s	585 Mb/s
DDR LVDS receiver (SPI-4.2)(1)	1.4 Gb/s	1.3 Gb/s	1.0 Gb/s	0.9 Gb/s
Maximum Physical Interface (PHY) Rate for Memory Interfaces(2)(3)				
DDR2	800 Mb/s	800 Mb/s	800 Mb/s	606 Mb/s
DDR3	1066 Mb/s	1066 Mb/s	800 Mb/s	606 Mb/s
QDR II + SRAM	400 MHz	350 MHz	300 MHz	–
RLDRAM II	500 MHz	400 MHz	350 MHz	–

Notes:

1. LVDS receivers are typically bounded with certain applications where specific DPA algorithms dominate deterministic performance.
2. Verified on Xilinx memory characterization platforms designed according to the guidelines in the *Virtex-6 FPGA Memory Interface Solutions User Guide*.
3. Consult the *Virtex-6 FPGA Memory Interface Solutions Data Sheet* for performance and feature information on memory interface cores (controller plus PHY).

Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.10 for -3, -2, and -1; and v1.07 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 42 correlates the current status of each Virtex-6 device on a per speed grade basis.

Table 42: **Virtex-6 Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC6VLX75T			-3, -2, -1, -1L
XC6VLX130T			-3, -2, -1, -1L
XC6VLX195T			-3, -2, -1, -1L
XC6VLX240T			-3, -2, -1, -1L
XC6VLX365T			-3, -2, -1, -1L
XC6VLX550T			-2, -1, -1L
XC6VLX760			-2, -1, -1L
XC6VSX315T			-3, -2, -1, -1L
XC6VSX475T			-2, -1, -1L
XC6VHX250T		-3, -2, -1	
XC6VHX255T	-3, -2, -1		
XC6VHX380T	-3, -2, -1		
XC6VHX565T	-2, -1		

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-6 devices.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 43 lists the production released Virtex-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE® software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 43: **Virtex-6 Device Production Software and Speed Specification Release**

Device	Speed Grade Designations			
	-3	-2	-1	-1L
XC6VLX75T	ISE 12.2 v1.08			ISE 12.3 v1.07 Patch
XC6VLX130T	ISE 12.1 v1.06	ISE 11.5 v1.05	ISE 11.5 v1.05	ISE 12.2 v1.05
XC6VLX195T	ISE 12.1 v1.06	ISE 12.1 v1.06	ISE 12.1 v1.06	ISE 12.2 v1.04
XC6VLX240T	ISE 12.1 v1.06	ISE 11.4.1 v1.04	ISE 11.4.1 v1.04	ISE 12.2 v1.04
XC6VLX365T	ISE 12.2 v1.08			ISE 12.2 v1.04
XC6VLX550T	N/A	ISE 12.2 v1.07		ISE 12.2 v1.04
XC6VLX760	N/A	ISE 12.2 v1.08		ISE 12.3 v1.07 Patch
XC6VSX315T	ISE 12.2 v1.08	ISE 12.1 v1.06		ISE 12.3 v1.07 Patch
XC6VSX475T	N/A	ISE 12.2 v1.08		ISE 12.3 v1.07 Patch
XC6VHX250T				N/A
XC6VHX255T				N/A
XC6VHX380T				N/A
XC6VHX565T	N/A			N/A

Notes:

1. Blank entries indicate a device and/or speed grade in advance or preliminary status.

IOB Pad Input/Output/3-State Switching Characteristics

Table 44 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 45 summarizes the value of T_{IOTPHZ}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 44: **IOB Switching Characteristics**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVDS_25	0.85	0.94	1.09	1.08	1.45	1.54	1.68	1.62	1.45	1.54	1.68	1.62	ns
LVDSEXT_25	0.85	0.94	1.09	1.08	1.53	1.65	1.84	1.73	1.53	1.65	1.84	1.73	ns
HT_25	0.85	0.94	1.09	1.08	1.51	1.62	1.78	1.69	1.51	1.62	1.78	1.69	ns

Table 44: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
BLVDS_25	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.65	1.39	1.50	1.67	1.65	ns
RSDS_25 (point to point)	0.85	0.94	1.09	1.08	1.45	1.54	1.68	1.62	1.45	1.54	1.68	1.62	ns
HSTL_I	0.81	0.91	1.06	1.06	1.45	1.56	1.73	1.71	1.45	1.56	1.73	1.71	ns
HSTL_II	0.81	0.91	1.06	1.06	1.44	1.56	1.74	1.72	1.44	1.56	1.74	1.72	ns
HSTL_III	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
HSTL_I_18	0.81	0.91	1.06	1.06	1.47	1.58	1.75	1.72	1.47	1.58	1.75	1.72	ns
HSTL_II_18	0.81	0.91	1.06	1.06	1.50	1.62	1.81	1.78	1.50	1.62	1.81	1.78	ns
HSTL_III_18	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
SSTL2_I	0.81	0.91	1.06	1.06	1.49	1.60	1.77	1.74	1.49	1.60	1.77	1.74	ns
SSTL2_II	0.81	0.91	1.06	1.06	1.42	1.54	1.72	1.71	1.42	1.54	1.72	1.71	ns
SSTL15	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
LVCMOS25, Slow, 2 mA	0.51	0.57	0.66	0.70	5.09	5.46	6.01	5.63	5.09	5.46	6.01	5.63	ns
LVCMOS25, Slow, 4 mA	0.51	0.57	0.66	0.70	3.30	3.49	3.79	3.65	3.30	3.49	3.79	3.65	ns
LVCMOS25, Slow, 6 mA	0.51	0.57	0.66	0.70	2.62	2.81	3.08	2.95	2.62	2.81	3.08	2.95	ns
LVCMOS25, Slow, 8 mA	0.51	0.57	0.66	0.70	2.21	2.41	2.72	2.59	2.21	2.41	2.72	2.59	ns
LVCMOS25, Slow, 12 mA	0.51	0.57	0.66	0.70	1.80	1.95	2.17	2.10	1.80	1.95	2.17	2.10	ns
LVCMOS25, Slow, 16 mA	0.51	0.57	0.66	0.70	1.89	2.05	2.29	2.21	1.89	2.05	2.29	2.21	ns
LVCMOS25, Slow, 24 mA	0.51	0.57	0.66	0.70	1.68	1.82	2.02	1.98	1.68	1.82	2.02	1.98	ns
LVCMOS25, Fast, 2 mA	0.51	0.57	0.66	0.70	5.12	5.49	6.04	5.62	5.12	5.49	6.04	5.62	ns
LVCMOS25, Fast, 4 mA	0.51	0.57	0.66	0.70	3.28	3.50	3.82	3.65	3.28	3.50	3.82	3.65	ns
LVCMOS25, Fast, 6 mA	0.51	0.57	0.66	0.70	2.56	2.73	2.99	2.88	2.56	2.73	2.99	2.88	ns
LVCMOS25, Fast, 8 mA	0.51	0.57	0.66	0.70	2.11	2.33	2.65	2.53	2.11	2.33	2.65	2.53	ns
LVCMOS25, Fast, 12 mA	0.51	0.57	0.66	0.70	1.74	1.88	2.08	2.03	1.74	1.88	2.08	2.03	ns
LVCMOS25, Fast, 16 mA	0.51	0.57	0.66	0.70	1.77	1.92	2.13	2.08	1.77	1.92	2.13	2.08	ns
LVCMOS25, Fast, 24 mA	0.51	0.57	0.66	0.70	1.66	1.79	1.99	1.96	1.66	1.79	1.99	1.96	ns
LVCMOS18, Slow, 2 mA	0.55	0.61	0.71	0.73	4.21	4.47	4.87	4.30	4.21	4.47	4.87	4.30	ns
LVCMOS18, Slow, 4 mA	0.55	0.61	0.71	0.73	2.79	2.96	3.21	2.94	2.79	2.96	3.21	2.94	ns
LVCMOS18, Slow, 6 mA	0.55	0.61	0.71	0.73	2.30	2.43	2.64	2.47	2.30	2.43	2.64	2.47	ns
LVCMOS18, Slow, 8 mA	0.55	0.61	0.71	0.73	2.01	2.11	2.27	2.24	2.01	2.11	2.27	2.24	ns
LVCMOS18, Slow, 12 mA	0.55	0.61	0.71	0.73	1.88	1.99	2.15	2.10	1.88	1.99	2.15	2.10	ns
LVCMOS18, Slow, 16 mA	0.55	0.61	0.71	0.73	1.84	1.95	2.11	2.04	1.84	1.95	2.11	2.04	ns
LVCMOS18, Fast, 2 mA	0.55	0.61	0.71	0.73	4.00	4.23	4.57	4.08	4.00	4.23	4.57	4.08	ns
LVCMOS18, Fast, 4 mA	0.55	0.61	0.71	0.73	2.62	2.76	2.97	2.74	2.62	2.76	2.97	2.74	ns
LVCMOS18, Fast, 6 mA	0.55	0.61	0.71	0.73	2.15	2.28	2.46	2.32	2.15	2.28	2.46	2.32	ns
LVCMOS18, Fast, 8 mA	0.55	0.61	0.71	0.73	1.90	1.99	2.13	2.14	1.90	1.99	2.13	2.14	ns
LVCMOS18, Fast, 12 mA	0.55	0.61	0.71	0.73	1.69	1.80	1.97	1.88	1.69	1.80	1.97	1.88	ns
LVCMOS18, Fast, 16 mA	0.55	0.61	0.71	0.73	1.63	1.74	1.91	1.88	1.63	1.74	1.91	1.88	ns
LVCMOS15, Slow, 2 mA	0.64	0.73	0.85	0.85	3.43	3.77	4.29	3.91	3.43	3.77	4.29	3.91	ns

Table 44: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVCMOS15, Slow, 4 mA	0.64	0.73	0.85	0.85	2.58	2.79	3.10	2.93	2.58	2.79	3.10	2.93	ns
LVCMOS15, Slow, 6 mA	0.64	0.73	0.85	0.85	2.08	2.32	2.68	2.50	2.08	2.32	2.68	2.50	ns
LVCMOS15, Slow, 8 mA	0.64	0.73	0.85	0.85	1.81	1.98	2.23	2.24	1.81	1.98	2.23	2.24	ns
LVCMOS15, Slow, 12 mA	0.64	0.73	0.85	0.85	1.76	1.91	2.13	2.07	1.76	1.91	2.13	2.07	ns
LVCMOS15, Slow, 16 mA	0.64	0.73	0.85	0.85	1.69	1.83	2.04	1.98	1.69	1.83	2.04	1.98	ns
LVCMOS15, Fast, 2 mA	0.64	0.73	0.85	0.85	3.44	3.77	4.28	3.91	3.44	3.77	4.28	3.91	ns
LVCMOS15, Fast, 4 mA	0.64	0.73	0.85	0.85	2.37	2.53	2.78	2.66	2.37	2.53	2.78	2.66	ns
LVCMOS15, Fast, 6 mA	0.64	0.73	0.85	0.85	1.80	2.05	2.42	2.16	1.80	2.05	2.42	2.16	ns
LVCMOS15, Fast, 8 mA	0.64	0.73	0.85	0.85	1.76	1.90	2.11	2.04	1.76	1.90	2.11	2.04	ns
LVCMOS15, Fast, 12 mA	0.64	0.73	0.85	0.85	1.64	1.77	1.97	1.90	1.64	1.77	1.97	1.90	ns
LVCMOS15, Fast, 16 mA	0.64	0.73	0.85	0.85	1.62	1.76	1.96	1.92	1.62	1.76	1.96	1.92	ns
LVCMOS12, Slow, 2 mA	0.72	0.81	0.93	0.95	3.14	3.39	3.75	3.54	3.14	3.39	3.75	3.54	ns
LVCMOS12, Slow, 4 mA	0.72	0.81	0.93	0.95	2.43	2.63	2.93	2.79	2.43	2.63	2.93	2.79	ns
LVCMOS12, Slow, 6 mA	0.72	0.81	0.93	0.95	1.92	2.11	2.41	2.26	1.92	2.11	2.41	2.26	ns
LVCMOS12, Slow, 8 mA	0.72	0.81	0.93	0.95	1.87	2.02	2.25	2.17	1.87	2.02	2.25	2.17	ns
LVCMOS12, Fast, 2 mA	0.72	0.81	0.93	0.95	2.71	2.98	3.39	3.11	2.71	2.98	3.39	3.11	ns
LVCMOS12, Fast, 4 mA	0.72	0.81	0.93	0.95	1.93	2.16	2.51	2.31	1.93	2.16	2.51	2.31	ns
LVCMOS12, Fast, 6 mA	0.72	0.81	0.93	0.95	1.75	1.89	2.11	2.05	1.75	1.89	2.11	2.05	ns
LVCMOS12, Fast, 8 mA	0.72	0.81	0.93	0.95	1.69	1.82	2.02	1.98	1.69	1.82	2.02	1.98	ns
LVDCI_25	0.51	0.57	0.66	0.70	2.05	2.14	2.26	2.26	2.05	2.14	2.26	2.26	ns
LVDCI_18	0.55	0.61	0.71	0.73	2.07	2.23	2.47	2.38	2.07	2.23	2.47	2.38	ns
LVDCI_15	0.64	0.73	0.85	0.85	1.85	2.01	2.24	2.18	1.85	2.01	2.24	2.18	ns
LVDCI_DV2_25	0.51	0.57	0.66	0.70	1.71	1.83	2.01	2.00	1.71	1.83	2.01	2.00	ns
LVDCI_DV2_18	0.55	0.61	0.71	0.73	1.69	1.81	2.00	1.98	1.69	1.81	2.00	1.98	ns
LVDCI_DV2_15	0.64	0.73	0.85	0.85	1.68	1.77	1.91	1.98	1.68	1.77	1.91	1.98	ns
LVPECL_25	0.85	0.94	1.09	1.08	1.38	1.49	1.65	1.64	1.38	1.49	1.65	1.64	ns
HSTL_I_12	0.81	0.91	1.06	1.06	1.48	1.60	1.78	1.74	1.48	1.60	1.78	1.74	ns
HSTL_I_DCI	0.81	0.91	1.06	1.06	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
HSTL_II_DCI	0.81	0.91	1.06	1.06	1.37	1.49	1.68	1.66	1.37	1.49	1.68	1.66	ns
HSTL_II_T_DCI	0.81	0.91	1.06	1.06	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
HSTL_III_DCI	0.81	0.91	1.06	1.06	1.34	1.45	1.62	1.61	1.34	1.45	1.62	1.61	ns
HSTL_I_DCI_18	0.81	0.91	1.06	1.06	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
HSTL_II_DCI_18	0.81	0.91	1.06	1.06	1.36	1.46	1.62	1.59	1.36	1.46	1.62	1.59	ns
HSTL_II _T_DCI_18	0.81	0.91	1.06	1.06	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
HSTL_III_DCI_18	0.81	0.91	1.06	1.06	1.43	1.54	1.69	1.67	1.43	1.54	1.69	1.67	ns
DIFF_HSTL_I_18	0.85	0.94	1.09	1.08	1.47	1.58	1.75	1.72	1.47	1.58	1.75	1.72	ns
DIFF_HSTL_I_DCI_18	0.85	0.94	1.09	1.08	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
DIFF_HSTL_I	0.85	0.94	1.09	1.08	1.45	1.56	1.73	1.71	1.45	1.56	1.73	1.71	ns

Table 44: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
DIFF_HSTL_I_DCI	0.85	0.94	1.09	1.08	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
DIFF_HSTL_II_18	0.85	0.94	1.09	1.08	1.50	1.62	1.81	1.78	1.50	1.62	1.81	1.78	ns
DIFF_HSTL_II_DCI_18	0.85	0.94	1.09	1.08	1.36	1.46	1.62	1.59	1.36	1.46	1.62	1.59	ns
DIFF_HSTL_II _T_DCI_18	0.85	0.94	1.09	1.08	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
DIFF_HSTL_II	0.85	0.94	1.09	1.08	1.44	1.56	1.74	1.72	1.44	1.56	1.74	1.72	ns
DIFF_HSTL_II_DCI	0.85	0.94	1.09	1.08	1.37	1.49	1.68	1.66	1.37	1.49	1.68	1.66	ns
SSTL2_I_DCI	0.81	0.91	1.06	1.06	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
SSTL2_II_DCI	0.81	0.91	1.06	1.06	1.39	1.50	1.67	1.69	1.39	1.50	1.67	1.69	ns
SSTL2_II_T_DCI	0.81	0.91	1.06	1.06	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
SSTL18_I	0.81	0.91	1.06	1.06	1.47	1.58	1.75	1.73	1.47	1.58	1.75	1.73	ns
SSTL18_II	0.81	0.91	1.06	1.06	1.39	1.50	1.67	1.66	1.39	1.50	1.67	1.66	ns
SSTL18_I_DCI	0.81	0.91	1.06	1.06	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
SSTL18_II_DCI	0.81	0.91	1.06	1.06	1.36	1.47	1.63	1.62	1.36	1.47	1.63	1.62	ns
SSTL18_II_T_DCI	0.81	0.91	1.06	1.06	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
SSTL15_T_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
SSTL15_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
DIFF_SSTL2_I	0.85	0.94	1.09	1.08	1.49	1.60	1.77	1.74	1.49	1.60	1.77	1.74	ns
DIFF_SSTL2_I_DCI	0.85	0.94	1.09	1.08	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
DIFF_SSTL2_II	0.85	0.94	1.09	1.08	1.42	1.54	1.72	1.71	1.42	1.54	1.72	1.71	ns
DIFF_SSTL2_II_DCI	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.69	1.39	1.50	1.67	1.69	ns
DIFF_SSTL2_II_T_DCI	0.85	0.94	1.09	1.08	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
DIFF_SSTL18_I	0.85	0.94	1.09	1.08	1.47	1.58	1.75	1.73	1.47	1.58	1.75	1.73	ns
DIFF_SSTL18_I_DCI	0.85	0.94	1.09	1.08	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
DIFF_SSTL18_II	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.66	1.39	1.50	1.67	1.66	ns
DIFF_SSTL18_II_DCI	0.85	0.94	1.09	1.08	1.36	1.47	1.63	1.62	1.36	1.47	1.63	1.62	ns
DIFF_SSTL18_II_T_DCI	0.85	0.94	1.09	1.08	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
DIFF_SSTL15	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
DIFF_SSTL15_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
DIFF_SSTL15_T_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns

Table 45: **IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{IOTPHZ}	T input to Pad high-impedance	0.86	0.92	0.99	0.99	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 46 shows the test setup parameters used for measuring input delay.

Table 46: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(5)	V_{REF} (1)(3)(5)
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL, Class III	HSTL_III	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	V_{REF} – 1.00	V_{REF} + 1.00	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	0(6)	–
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	0(6)	–
HT (HyperTransport), 2.5V	LDT_25	0.6 – 0.125	0.6 + 0.125	0(6)	–

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVCMOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 6.
6. The value given is the differential input voltage.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 6 and Figure 7.

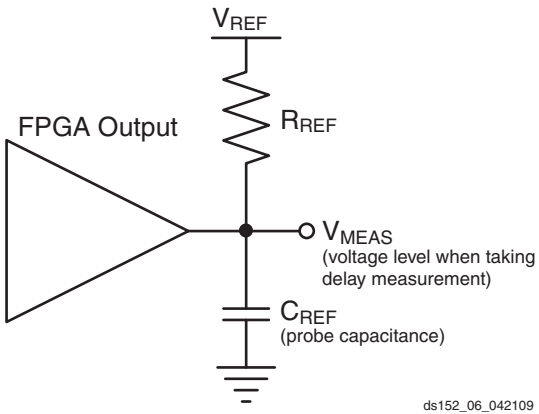

Figure 6: **Single Ended Test Setup**

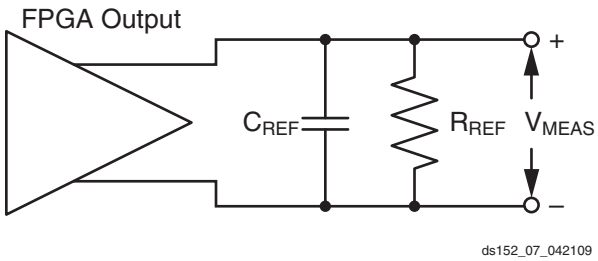

Figure 7: **Differential Test Setup**

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 47.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 47: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.2V	LVCMOS12	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	100	0	0[2]	1.2
LVDSEXT (LVDS Extended Mode), 2.5V	LVDS_25	100	0	0[2]	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0[2]	0

Table 47: **Output Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
HT (HyperTransport), 2.5V	LDT_25	100	0	0[2]	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	100	0	0[2]	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V_{REF}	0.75
HSTL, Class III, with DCI	HSTL_III_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V_{REF}	0.9
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termi.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V_{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V_{REF}	1.25

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 48: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Setup/Hold						
T_{ICE1CK}/T_{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.21/ 0.03	0.25/ 0.04	0.27/ 0.04	0.31/ 0.05	ns
T_{ISRCK}/T_{ICKSR}	SR pin Setup/Hold with respect to CLK	0.66/ –0.08	0.78/ –0.08	0.96/ –0.08	1.09/ –0.11	ns
T_{IDOCK}/T_{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	0.07/ 0.41	0.08/ 0.46	0.10/ 0.54	0.11/ 0.64	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.10/ 0.32	0.12/ 0.36	0.14/ 0.42	0.16/ 0.50	ns
Combinatorial						
T_{IDI}	D pin to O pin propagation delay, no Delay	0.15	0.17	0.20	0.23	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IODELAY)	0.19	0.22	0.25	0.28	ns
Sequential Delays						
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.48	0.54	0.64	0.73	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY)	0.52	0.58	0.68	0.78	ns
T_{ICKQ}	CLK to Q outputs	0.54	0.61	0.70	0.93	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out	0.85	0.97	1.15	1.32	ns
T_{GSRQ_ILOGIC}	Global Set/Reset to Q outputs	7.60	7.60	10.51	10.51	ns
Set/Reset						
T_{RPW_ILOGIC}	Minimum Pulse Width, SR inputs	0.78	0.95	1.20	1.30	ns, Min

Table 49: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Setup/Hold						
T_{ODCK}/T_{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.45/ –0.08	0.50/ –0.08	0.54/ –0.08	0.69/ –0.11	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.17/ –0.03	0.20/ –0.03	0.22/ –0.03	0.27/ –0.04	ns
T_{OSRCK}/T_{OCKSR}	SR pin Setup/Hold with respect to CLK	0.59/ –0.24	0.62/ –0.24	0.71/ –0.24	0.79/ –0.35	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.44/ –0.07	0.51/ –0.07	0.56/ –0.07	0.68/ –0.13	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.15/ –0.04	0.19/ –0.04	0.21/ –0.04	0.29/ –0.05	ns
Combinatorial						
T_{DOQ}	D1 to OQ out or T1 to TQ out	0.78	0.87	1.01	1.15	ns
Sequential Delays						
T_{OCKQ}	CLK to OQ/TQ out	0.54	0.61	0.71	0.80	ns
T_{RQ}	SR pin to OQ/TQ out	0.80	0.90	1.05	1.19	ns
T_{GSRQ}	Global Set/Reset to Q outputs	7.60	7.60	10.51	10.51	ns
Set/Reset						
T_{RPW}	Minimum Pulse Width, SR inputs	0.78	0.95	1.20	1.30	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 50: **ISERDES Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Setup/Hold for Control Lines						
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.07/ 0.15	0.08/ 0.16	0.09/ 0.17	0.14/ 0.17	ns
T_{ISCCK_CE} / T_{ISCKC_CE}(2)	CE pin Setup/Hold with respect to CLK (for CE1)	0.20/ 0.03	0.25/ 0.04	0.27/ 0.04	0.31/ 0.05	ns
T_{ISCCK_CE2} / T_{ISCKC_CE2}(2)	CE pin Setup/Hold with respect to CLKDIV (for CE2)	0.01/ 0.27	0.01 0.29	0.01/ 0.31	–0.05/ 0.35	ns
Setup/Hold for Data Lines						
T_{ISDCK_D} /T_{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.07/ 0.08	0.08/ 0.09	0.09/ 0.11	0.11/ 0.19	ns
T_{ISDCK_DDLY} /T_{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)(1)	0.10/ 0.05	0.12/ 0.06	0.14/ 0.07	0.16/ 0.15	ns
$T_{ISDCK\_D\_DDR}$ /$T_{ISCKD\_D\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode	0.07/ 0.08	0.08/ 0.09	0.09/ 0.11	0.11/ 0.19	ns
$T_{ISDCK\_DDLY\_DDR}$ $T_{ISCKD\_DDLY\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY)(1)	0.10/ 0.05	0.12/ 0.06	0.14/ 0.07	0.16/ 0.15	ns
Sequential Delays						
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.57	0.66	0.75	0.88	ns
Propagation Delays						
T_{ISDO_DO}	D input to DO output pin	0.19	0.22	0.25	0.28	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as T_{ISCCK_CE}/T_{ISCKC_CE} in TRACE report.

Output Serializer/Deserializer Switching Characteristics

Table 51: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Setup/Hold						
T_{OSDCK_D}/T_{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.23/ –0.10	0.28/ –0.10	0.31/ –0.10	0.36/ –0.15	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input Setup/Hold with respect to CLK	0.44/ –0.10	0.51/ –0.09	0.56/ –0.08	0.68/ –0.15	ns
$T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1)	T input Setup/Hold with respect to CLKDIV	0.25/ –0.10	0.27/ –0.09	0.31/ –0.08	0.47/ –0.15	ns
$T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$	OCE input Setup/Hold with respect to CLK	0.17/ –0.03	0.20/ –0.03	0.22/ –0.03	0.27/ –0.04	ns
T_{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV	0.07	0.07	0.07	0.08	ns
$T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$	TCE input Setup/Hold with respect to CLK	0.15/ –0.04	0.19/ –0.04	0.21/ –0.04	0.29/ –0.05	ns
Sequential Delays						
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.63	0.71	0.82	0.93	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.63	0.71	0.82	0.93	ns
Combinatorial						
T_{OSDO_TTQ}	T input to TQ Out	0.76	0.84	0.97	1.11	ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

Input/Output Delay Switching Characteristics

Table 52: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
IDELAYCTRL						
T_{DLYCCO_RDY}	Reset to Ready for IDELAYCTRL	3.00	3.00	3.00	3.25	µs
$F_{IDELAYCTRL\_REF}$	Attribute REFCLK frequency = 200.0(1)	200	200	200	200	MHz
	Attribute REFCLK frequency = 300.0(1)	300	300	–	–	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum Reset pulse width	50.00	50.00	50.00	52.50	ns
IODELAY						
$T_{IDELAYRESOLUTION}$	IODELAY Chain Delay Resolution	$1/(32 \times 2 \times F_{REF})$				ps
$T_{IDELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern.(2)	0	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).(3)	±5	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).(4)	±9	±9	±9	±9	ps per tap
$T_{IODELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IODELAY	500.00	420.00	300.00	300.00	MHz
T_{IODCCK_CE} / T_{IODCKC_CE}	CE pin Setup/Hold with respect to CK	0.45/ –0.09	0.53/ –0.09	0.65/ –0.09	0.84/ –0.14	ns
T_{IODCK_INC}/ T_{IODCKC_INC}	INC pin Setup/Hold with respect to CK	0.23/ –0.02	0.27/ –0.01	0.31/ 0.00	0.27/ –0.04	ns
T_{IODCCK_RST}/ T_{IODCKC_RST}	RST pin Setup/Hold with respect to CK	0.57/ –0.08	0.62/ –0.08	0.69/ –0.08	0.74/ –0.13	ns
T_{IODDO_T}	TSCONTROL delay to MUXE/MUXF switching and through IODELAY	Note 5	Note 5	Note 5	Note 5	ps
$T_{IODDO\_IDATAIN}$	Propagation delay through IODELAY	Note 5	Note 5	Note 5	Note 5	ps
$T_{IODDO\_ODATAIN}$	Propagation delay through IODELAY	Note 5	Note 5	Note 5	Note 5	ps

Notes:

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IODELAY tap setting. See TRACE report for actual values.

CLB Switching Characteristics

Table 53: **CLB Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Combinatorial Delays						
T_{ILO}	An – Dn LUT address to A	0.06	0.07	0.07	0.09	ns, Max
	An – Dn LUT address to AMUX/CMUX	0.18	0.20	0.22	0.25	ns, Max
	An – Dn LUT address to BMUX_A	0.28	0.31	0.36	0.40	ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs	0.59	0.67	0.79	0.85	ns, Max
T_{AXA}	AX inputs to AMUX output	0.31	0.35	0.42	0.44	ns, Max
T_{AXB}	AX inputs to BMUX output	0.35	0.39	0.47	0.50	ns, Max
T_{AXC}	AX inputs to CMUX output	0.39	0.44	0.52	0.56	ns, Max
T_{AXD}	AX inputs to DMUX output	0.42	0.47	0.55	0.60	ns, Max
T_{BXB}	BX inputs to BMUX output	0.30	0.34	0.39	0.44	ns, Max
T_{BXD}	BX inputs to DMUX output	0.38	0.43	0.50	0.55	ns, Max
T_{CXB}	CX inputs to CMUX output	0.26	0.29	0.34	0.37	ns, Max
T_{CXD}	CX inputs to DMUX output	0.30	0.34	0.40	0.44	ns, Max
T_{DXD}	DX inputs to DMUX output	0.30	0.33	0.38	0.43	ns, Max
T_{OPCYA}	An input to COUT output	0.32	0.36	0.41	0.47	ns, Max
T_{OPCYB}	Bn input to COUT output	0.32	0.36	0.41	0.47	ns, Max
T_{OPCYC}	Cn input to COUT output	0.27	0.30	0.34	0.40	ns, Max
T_{OPCYD}	Dn input to COUT output	0.25	0.28	0.32	0.37	ns, Max
T_{AXCY}	AX input to COUT output	0.25	0.28	0.33	0.36	ns, Max
T_{BXCY}	BX input to COUT output	0.22	0.24	0.28	0.31	ns, Max
T_{CXCY}	CX input to COUT output	0.15	0.17	0.20	0.22	ns, Max
T_{DXCY}	DX input to COUT output	0.14	0.16	0.19	0.21	ns, Max
T_{BYP}	CIN input to COUT output	0.06	0.07	0.08	0.09	ns, Max
T_{CINA}	CIN input to AMUX output	0.21	0.24	0.28	0.30	ns, Max
T_{CINB}	CIN input to BMUX output	0.23	0.25	0.29	0.31	ns, Max
T_{CINC}	CIN input to CMUX output	0.23	0.26	0.30	0.33	ns, Max
T_{CIND}	CIN input to DMUX output	0.25	0.29	0.33	0.36	ns, Max
Sequential Delays						
T_{CKO}	Clock to AQ – DQ outputs	0.29	0.33	0.39	0.44	ns, Max
T_{SHCKO}	Clock to AMUX – DMUX outputs	0.36	0.40	0.47	0.53	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T_{DICK}/T_{CKDI}	A – D input to CLK on A – D Flip Flops	0.30/ 0.17	0.36/ 0.18	0.43/ 0.20	0.44/ 0.25	ns, Min
T_{CECK_CLB}/ T_{CKCE_CLB}	CE input to CLK on A – D Flip Flops	0.20/ 0.00	0.25/ 0.00	0.32/ 0.00	0.32/ 0.01	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D Flip Flops	0.39/ –0.07	0.44/ –0.07	0.52/ –0.07	0.58/ –0.08	ns, Min
T_{CINCK}/T_{CKCIN}	CIN input to CLK on A – D Flip Flops	0.16/ 0.12	0.19/ 0.14	0.24/ 0.16	0.23/ 0.22	ns, Min

Table 53: **CLB Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Set/Reset						
T_{SRMIN}	SR input minimum pulse width	0.90	0.90	0.97	0.80	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops	0.52	0.58	0.68	0.77	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.41	0.48	0.59	0.61	ns, Max
F_{TOG}	Toggle frequency (for export control)	1412.00	1286.40	1098.00	1098.00	MHz

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. These items are of interest for Carry Chain applications.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 54: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Sequential Delays						
T_{SHCKO}	Clock to A – B outputs	0.92	1.10	1.36	1.49	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	1.19	1.40	1.71	1.87	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{DS}/T_{DH}	A – D inputs to CLK	0.62/ 0.18	0.72/ 0.20	0.88/ 0.22	0.98/ 0.23	ns, Min
T_{AS}/T_{AH}	Address An inputs to clock	0.19/ 0.52	0.22/ 0.59	0.27/ 0.66	0.30/ 0.75	ns, Min
T_{WS}/T_{WH}	WE input to clock	0.27/ 0.00	0.32/ 0.00	0.40/ 0.00	0.47/ –0.03	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.28/ –0.01	0.34/ –0.01	0.41/ –0.01	0.48/ –0.05	ns, Min
Clock CLK						
T_{MPW}	Minimum pulse width	0.70	0.82	1.00	1.04	ns, Min
T_{MCP}	Minimum clock period	1.40	1.64	2.00	2.08	ns, Min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 55: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Sequential Delays						
T_{REG}	Clock to A – D outputs	1.11	1.30	1.58	1.74	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	1.37	1.60	1.93	2.12	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	1.08	1.27	1.55	1.74	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{WS}/T_{WH}	WE input	0.05/ 0.00	0.07/ 0.00	0.09/ 0.00	0.11/ 0.03	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.06/ –0.01	0.08/ –0.01	0.10/ –0.01	0.12/ 0.02	ns, Min
T_{DS}/T_{DH}	A – D inputs to CLK	0.64/ 0.18	0.76/ 0.21	0.94/ 0.24	1.07/ 0.23	ns, Min
Clock CLK						
T_{MPW}	Minimum pulse width	0.60	0.70	0.85	0.89	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Block RAM and FIFO Switching Characteristics

Table 56: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Block RAM and FIFO Clock-to-Out Delays						
T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$[1]	Clock CLK to DOUT output (without output register)[2][3]	1.60	1.79	2.08	2.36	ns, Max
	Clock CLK to DOUT output (with output register)[4][5]	0.60	0.66	0.75	0.83	ns, Max
$T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$	Clock CLK to DOUT output with ECC (without output register)[2][3]	2.62	2.89	3.30	3.73	ns, Max
	Clock CLK to DOUT output with ECC (with output register)[4][5]	0.71	0.77	0.86	0.94	ns, Max
T_{RCKO_CASC} and $T_{RCKO\_CASC\_REG}$	Clock CLK to DOUT output with Cascade (without output register)[2]	2.49	2.77	3.18	3.61	ns, Max
	Clock CLK to DOUT output with Cascade (with output register)[4]	1.29	1.41	1.58	1.79	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs[6]	0.74	0.81	0.91	0.98	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointers outputs[7]	0.90	0.98	1.09	1.21	ns, Max
$T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$	Clock CLK to BITERR (with output register)	0.62	0.68	0.76	0.82	ns, Max
	Clock CLK to BITERR (without output register)	2.21	2.46	2.84	3.23	ns, Max
$T_{RCKO\_PARITY\_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode	0.86	0.94	1.06	1.18	ns, Max
$T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$	Clock CLK to RDADDR output with ECC (without output register)	0.73	0.79	0.90	1.00	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.76	0.82	0.92	1.02	ns, Max
Setup and Hold Times Before/After Clock CLK						
$T_{RCCK\_ADDR}/T_{RCKC\_ADDR}$	ADDR inputs[8]	0.47/ 0.27	0.53/ 0.29	0.62/ 0.32	0.66/ 0.34	ns, Min
T_{RDCK_DI}/T_{RCKD_DI}	DIN inputs[9]	0.84/ 0.30	0.95/ 0.32	1.11/ 0.34	1.26/ 0.36	ns, Min
$T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$	DIN inputs with block RAM ECC in standard mode[9]	0.47/ 0.30	0.52/ 0.32	0.59/ 0.34	0.68/ 0.36	ns, Min
	DIN inputs with block RAM ECC encode only[9]	0.68/ 0.30	0.75/ 0.32	0.85/ 0.34	0.97/ 0.36	ns, Min
	DIN inputs with FIFO ECC in standard mode[9]	0.77/ 0.30	0.87/ 0.32	1.02/ 0.34	1.16/ 0.36	ns, Min
$T_{RCCK\_CLK}/T_{RCKC\_CLK}$	Inject single/double bit error in ECC mode	0.90/ 0.27	1.02/ 0.28	1.20/ 0.29	1.56/ 0.29	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	Block RAM Enable (EN) input	0.31/ 0.26	0.35/ 0.27	0.41/ 0.30	0.44/ 0.31	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.18/ 0.25	0.19/ 0.27	0.22/ 0.31	0.24/ 0.33	ns, Min
$T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$	Synchronous RSTREG input	0.22/ 0.23	0.24/ 0.24	0.28/ 0.26	0.31/ 0.27	ns, Min
$T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$	Synchronous RSTRAM input	0.32/ 0.23	0.36/ 0.24	0.41/ 0.27	0.46/ 0.29	ns, Min

Table 56: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{RCCK_WE}/T_{RCKC_WE}	Write Enable (WE) input (Block RAM only)	0.44/ 0.19	0.47/ 0.25	0.52/ 0.35	0.67/ 0.24	ns, Min
$T_{RCCK\_WREN}/T_{RCKC\_WREN}$	WREN FIFO inputs	0.47/ 0.26	0.50/ 0.27	0.55/ 0.30	0.68/ 0.31	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	RDEN FIFO inputs	0.46/ 0.26	0.50/ 0.27	0.55/ 0.30	0.67/ 0.31	ns, Min
Reset Delays						
T_{RCO_FLAGS}	Reset RST to FIFO Flags/Pointers(10)	0.90	0.98	1.10	1.23	ns, Max
$T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$	FIFO reset timing(11)	0.22/ 0.23	0.24/ 0.24	0.28/ 0.26	0.31/ 0.27	ns, Min
Maximum Frequency						
F_{MAX}	Block RAM (Write First and No Change modes)	600	540	450	340	MHz
	Block RAM (Read First mode)	525	475	400	275	MHz
	Block RAM (SDP mode)	525	475	400	275	MHz
$F_{MAX\_CASCADE}$	Block RAM Cascade (Write First and No Change modes)	550	490	400	300	MHz
	Block RAM Cascade (Read First mode)	475	425	350	235	MHz
F_{MAX_FIFO}	FIFO in all modes	600	540	450	340	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	450	400	325	250	MHz

Notes:

1. TRACE will report all of these parameters as T_{RCKO_DO}.
2. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. T_{RCKO_DI} includes both A and B inputs as well as the parity inputs of A and B.
10. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. The FIFO reset must be asserted for at least three positive clock edges.

DSP48E1 Switching Characteristics

Table 57: **DSP48E1 Switching Characteristics**

Symbol	Description	Speed				Units
		-3	-2	-1	-1L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock						
$T_{DSPDCK\_\{A, ACIN; B, BCIN\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{A, ACIN; B, BCIN\}\_\{AREG; BREG\}}$	{A, ACIN, B, BCIN} input to {A, B} register CLK	0.25/ 0.27	0.29/ 0.30	0.35/ 0.34	0.46/ 0.39	ns
$T_{DSPDCK\_C\_CREG}/T_{DSPCKD\_C\_CREG}$	C input to C register CLK	0.16/ 0.20	0.19/ 0.22	0.22/ 0.24	0.33/ 0.30	ns
$T_{DSPDCK\_D\_DREG}/T_{DSPCKD\_D\_DREG}$	D input to D register CLK	0.07/ 0.31	0.10/ 0.34	0.15/ 0.39	0.24/ 0.45	ns

Table 57: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed				Units
		-3	-2	-1	-1L	
Setup and Hold Times of Data Pins to the Pipeline Register Clock						
$T_{DSPDCK\_\{A, ACIN, B, BCIN\}\_MREG\_MULT}$/ $T_{DSPCKD\_\{A, ACIN, B, BCIN\}\_MREG\_MULT}$	{A, ACIN, B, BCIN} input to M register CLK	2.36/ 0.04	2.70/ 0.04	3.21/ 0.04	3.66/ 0.02	ns
$T_{DSPDCK\_\{A, D\}\_ADREG}$/ $T_{DSPCKD\_\{A, D\}\_ADREG}$	{A, D} input to AD register CLK	1.24/ 0.10	1.42/ 0.12	1.69/ 0.13	1.91/ 0.16	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock						
$T_{DSPDCK\_\{A, ACIN, B, BCIN\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, ACIN, B, BCIN\}\_PREG\_MULT}$	{A, ACIN, B, BCIN} input to P register CLK using multiplier	3.83/ –0.13	4.37/ –0.13	5.20/ –0.13	5.94/ –0.24	ns
$T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$	D input to P register CLK	3.62/ –0.47	4.13/ –0.47	4.90/ –0.47	5.61/ –0.77	ns
$T_{DSPDCK\_\{A, ACIN, B, BCIN\}\_PREG}$/ $T_{DSPCKD\_\{A, ACIN, B, BCIN\}\_PREG}$	{A, ACIN, B, BCIN} input to P register CLK not using multiplier	1.59/ –0.13	1.81/ –0.13	2.15/ –0.13	2.44/ –0.24	ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK	1.42/ –0.10	1.61/ –0.10	1.91/ –0.10	2.16/ –0.19	ns
$T_{DSPDCK\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_PREG}$/ $T_{DSPCKD\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_PREG}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK	1.23/ –0.02	1.41/ –0.02	1.67/ –0.02	1.91/ –0.07	ns
Setup and Hold Times of the CE Pins						
$T_{DSPDCK\_\{CEA; CEB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{CEA; CEB\}\_\{AREG; BREG\}}$	{CEA; CEB} input to {A; B} register CLK	0.14/ 0.19	0.17/ 0.22	0.22/ 0.25	0.30/ 0.28	ns
$T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$	CEC input to C register CLK	0.15/ 0.18	0.18/ 0.20	0.24/ 0.23	0.31/ 0.26	ns
$T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$	CED input to D register CLK	0.20/ 0.12	0.24/ 0.13	0.31/ 0.14	0.43/ 0.16	ns
$T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK	0.16/ 0.19	0.20/ 0.21	0.26/ 0.25	0.32/ 0.28	ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK	0.32/ 0.02	0.38/ 0.02	0.46/ 0.03	0.54/ 0.04	ns
Setup and Hold Times of the RST Pins						
$T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK	0.27/ 0.17	0.31/ 0.19	0.38/ 0.22	0.41/ 0.25	ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK	0.18/ 0.08	0.20/ 0.08	0.23/ 0.09	0.27/ 0.11	ns
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.28/ 0.15	0.32/ 0.16	0.38/ 0.19	0.45/ 0.21	ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.20/ 0.24	0.23/ 0.26	0.26/ 0.30	0.29/ 0.34	ns
$T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.26/ 0.04	0.30/ 0.04	0.35/ 0.05	0.43/ 0.06	ns
Combinatorial Delays from Input Pins to Output Pins						
$T_{DSPDO\_\{A, B\}\_\{P, CARRYOUT\}\_MULT}$	{A, B} input to {P, CARRYOUT} output using multiplier	3.76	4.29	5.08	5.87	ns
$T_{DSPDO\_D\_\{P, CARRYOUT\}\_MULT}$	D input to {P, CARRYOUT} output using multiplier	3.57	4.07	4.82	5.57	ns
$T_{DSPDO\_\{A, B\}\_\{P, CARRYOUT\}}$	{A, B} input to {P, CARRYOUT} output not using multiplier	1.55	1.76	2.07	2.41	ns
$T_{DSPDO\_\{C, CARRYIN\}\_\{P, CARRYOUT\}}$	{C, CARRYIN} input to {P, CARRYOUT} output	1.38	1.56	1.83	2.13	ns

Table 57: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed				Units
		-3	-2	-1	-1L	
Combinatorial Delays from Input Pins to Cascading Output Pins						
$T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.49	0.56	0.65	0.73	ns
$T_{DSPDO\_\{A, B\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.87	4.42	5.24	6.09	ns
$T_{DSPDO\_D\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$	D input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.66	4.17	4.94	5.76	ns
$T_{DSPDO\_\{A, B\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	1.64	1.86	2.19	2.60	ns
$T_{DSPDO\_\_\{C, CARRYIN\}\_\{PCOUT, CARRYCASCOUT,MULTSIGNOUT\}}$	{C, CARRYIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.46	1.66	1.95	2.32	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins						
$T_{DSPDO\_\{ACIN, BCIN\}\_\{P, CARRYOUT\}\_MULT}$	{ACIN, BCIN} input to {P, CARRYOUT} output using multiplier	3.67	4.19	4.97	5.75	ns
$T_{DSPDO\_\{ACIN, BCIN\}\_\{P, CARRYOUT}$	{ACIN, BCIN} input to {P, CARRYOUT} output not using multiplier	1.43	1.63	1.92	2.25	ns
$T_{DSPDO\_\{ACIN; BCIN\}\_\{ACOUT; BCOUT\}}$	{ACIN, BCIN} input to {ACOUT, BCOUT} output	0.36	0.42	0.49	0.56	ns
$T_{DSPDO\_\{ACIN, BCIN\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.76	4.29	5.10	5.94	ns
$T_{DSPDO\_\{ACIN, BCIN\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	1.52	1.73	2.05	2.44	ns
$T_{DSPDO\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_\{P, CARRYOUT\}}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {P, CARRYOUT} output	1.19	1.35	1.60	1.87	ns
$T_{DSPDO\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.28	1.46	1.72	2.06	ns
Clock to Outs from Output Register Clock to Output Pins						
$T_{DSPCKO\_\{P, CARRYOUT\}\_PREG}$	CLK (PREG) to {P, CARRYOUT} output	0.38	0.43	0.50	0.57	ns
$T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_PREG}$	CLK (PREG) to {CARRYCASCOUT, PCOUT, MULTSIGNOUT} output	0.50	0.56	0.66	0.76	ns
Clock to Outs from Pipeline Register Clock to Output Pins						
$T_{DSPCKO\_\{P, CARRYOUT\}\_MREG}$	CLK (MREG) to {P, CARRYOUT} output	1.72	1.96	2.30	2.69	ns
$T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MREG}$	CLK (MREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.81	2.06	2.43	2.88	ns
$T_{DSPCKO\_\{P, CARRYOUT\}\_ADREG\_MULT}$	CLK (ADREG) to {P, CARRYOUT} output	2.79	3.16	3.72	4.32	ns
$T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_ADREG\_MULT}$	CLK (ADREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	2.87	3.26	3.84	4.51	ns

Table 57: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed				Units
		-3	-2	-1	-1L	
Clock to Outs from Input Register Clock to Output Pins						
$T_{DSPCKO\_\{P, CARRYOUT\}\_\{AREG, BREG\}\_MULT}$	CLK (AREG, BREG) to {P, CARRYOUT} output using multiplier	3.97	4.52	5.36	6.20	ns
$T_{DSPCKO\_\{P, CARRYOUT\}\_\{AREG, BREG\}}$	CLK (AREG, BREG) to {P, CARRYOUT} output not using multiplier	1.70	1.93	2.27	2.65	ns
$T_{DSPCKO\_\{P, CARRYOUT\}\_CREG}$	CLK (CREG) to {P, CARRYOUT} output	1.70	1.93	2.27	2.80	ns
$T_{DSPCKO\_\{P, CARRYOUT\}\_DREG\_MULT}$	CLK (DREG) to {P, CARRYOUT} output	3.89	4.44	5.25	6.07	ns
Clock to Outs from Input Register Clock to Cascading Output Pins						
$T_{DSPCKO\_\{ACOUT; BCOUT\}\_\{AREG; BREG\}}$	CLK (AREG, BREG) to {P, CARRYOUT} output	0.66	0.76	0.89	1.01	ns
$T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_\{AREG, BREG\}\_MULT}$	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	4.05	4.63	5.49	6.39	ns
$T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_\{AREG, BREG\}}$	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	1.79	2.03	2.40	2.84	ns
$T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_DREG\_MULT}$	CLK (DREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.98	4.54	5.38	6.26	ns
$T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_CREG}$	CLK (CREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.78	2.03	2.40	2.99	ns
Maximum Frequency						
F_{MAX}	With all registers used	600	540	450	410	MHz
F_{MAX_PATDET}	With pattern detector	551	483	408	356	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	356	311	262	224	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	327	286	241	211	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG	398	347	292	254	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect	398	347	292	254	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	266	233	196	171	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	250	219	184	160	MHz

Configuration Switching Characteristics

Table 58: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Power-up Timing Characteristics						
T_{PL} (1)	Program Latency	5	5	5	5	ms, Max
T_{POR} (1)	Power-on-Reset	15/55	15/55	15/55	15/55	ms, Min/Max
T_{ICCK}	CCLK (output) delay	400	400	400	400	ns, Min
$T_{PROGRAM}$	Program Pulse Width	250	250	250	250	ns, Min

Table 58: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Master/Slave Serial Mode Programming Switching						
T_{DCCK}/T_{CCKD}	DIN Setup/Hold, slave mode	4.0/0.0	4.0/0.0	4.0/0.0	4.5/0.0	ns, Min
T_{DSCCK}/T_{SCCKD}	DIN Setup/Hold, master mode	4.0/0.0	4.0/0.0	4.0/0.0	5.0/0.0	ns, Min
T_{CCO}	DOUT at 2.5V	6	6	6	7	ns, Max
	DOUT at 1.8V	6	6	6	7	ns, Max
F_{MCCK}	Maximum CCLK frequency, serial modes	100	100	100	100	MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance, master mode with respect to nominal CCLK.	55	55	55	55	%
F_{MSCCK}	Slave mode external CCLK	100	100	100	100	MHz
SelectMAP Mode Programming Switching						
T_{SMDCCK}/T_{SMCCKD}	SelectMAP Data Setup/Hold	4.0/0.0	4.0/0.0	4.0/0.0	5.5/0.0	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B Setup/Hold	4.0/0.0	4.0/0.0	4.0/0.0	4.5/0.0	ns, Min
T_{SMCCKW}/T_{SMWCCK}	RDWR_B Setup/Hold	10.0/0.0	10.0/0.0	10.0/0.0	13.5/0.0	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330 Ω pull-up resistor required)	6	6	6	7	ns, Min
T_{SMCO}	CCLK to DATA out in readback at 2.5V	6	6	6	7	ns, Max
	CCLK to DATA out in readback at 1.8V	6	6	6	7	ns, Max
T_{SMCKBY}	CCLK to BUSY out in readback at 2.5V	6	6	6	7	ns, Max
	CCLK to BUSY out in readback at 1.8V	6	6	6	7	ns, Max
F_{SMCCK}	Maximum Frequency with respect to nominal CCLK	100	100	100	70	MHz, Max
F_{RBCCK}	Maximum Readback Frequency with respect to nominal CCLK	100	100	100	100	MHz, Max
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK	55	55	55	55	%
Boundary-Scan Port Timing Specifications						
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI Setup time before TCK/ Hold time after TCK	3.0/2.0	3.0/2.0	3.0/2.0	4.0/2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output valid at 2.5V	6	6	6	7	ns, Max
	TCK falling edge to TDO output valid at 1.8V	6	6	6	7	ns, Max
F_{TCK}	Maximum configuration TCK clock frequency	66	66	66	66	MHz, Max
F_{TCKB_MIN}	Minimum boundary-scan TCK clock frequency when using IEEE Std 1149.6 (AC-JTAG). Minimum operating temperature for IEEE Std 1149.6 is 0°C.	15	15	15	15	MHz, Min
F_{TCKB}	Maximum boundary-scan TCK clock frequency	66	66	66	66	MHz, Max

Table 58: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
BPI Master Flash Mode Programming Switching						
T_{BPICCO}[2]	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge at 2.5V	6	6	6	7	ns
	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge at 1.8V	6	6	6	7	ns
T_{BPIDCC}/T_{BPICCD}	Setup/Hold on D[15:0] data input pins	4.0/0.0	4.0/0.0	4.0/0.0	5.0/0.0	ns
$T_{INITADDR}$	Minimum period of initial ADDR[25:0] address cycles	3	3	3	3	CCLK cycles
SPI Master Flash Mode Programming Switching						
$T_{SPIDCC}/T_{SPIDCCD}$	DIN Setup/Hold before/after the rising CCLK edge	3.0/0.0	3.0/0.0	3.0/0.0	3.5/0.0	ns
T_{SPICCM}	MOSI clock to out at 2.5V	6	6	6	7	ns
	MOSI clock to out at 1.8V	6	6	6	7	ns
$T_{SPICCFC}$	FCS_B clock to out at 2.5V	6	6	6	7	ns
	FCS_B clock to out at 1.8V	6	6	6	7	ns
$T_{FSINIT}/T_{FSINITH}$	FS[2:0] to INIT_B rising edge Setup and Hold	2	2	2	2	µs
CCLK Output (Master Modes)						
T_{MCCKL}	Master CCLK clock Low time duty cycle	45/55	45/55	45/55	45/55	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle	45/55	45/55	45/55	45/55	%, Min/Max
CCLK Input (Slave Modes)						
T_{SCCKL}	Slave CCLK clock minimum Low time	2.5	2.5	2.5	2.5	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time	2.5	2.5	2.5	2.5	ns, Min
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK						
F_{DCK}	Maximum frequency for DCLK	200	200	200	200	MHz
$T_{MMCMDCK\_DADDR}/T_{MMCMCKD\_DADDR}$	DADDR Setup/Hold	1.25/0.00	1.40/0.00	1.63/0.00	1.64/0.00	ns
$T_{MMCMDCK\_DI}/T_{MMCMCKD\_DI}$	DI Setup/Hold	1.25/0.00	1.40/0.00	1.63/0.00	1.64/0.00	ns
$T_{MMCMDCK\_DEN}/T_{MMCMCKD\_DEN}$	DEN Setup/Hold time	1.25/0.00	1.40/0.00	1.63/0.00	1.64/0.00	ns
$T_{MMCMDCK\_DWE}/T_{MMCMCKD\_DWE}$	DWE Setup/Hold time	1.25/0.00	1.40/0.00	1.63/0.00	1.64/0.00	ns
$T_{MMCMCKO\_DO}$	CLK to out of DO[3]	2.60	3.02	3.64	3.68	ns
$T_{MMCMCKO\_DRDY}$	CLK to out of DRDY	0.32	0.34	0.38	0.38	ns

Notes:

1. To support longer delays in configuration, use the design solutions described in *Virtex-6 FPGA Configuration User Guide*.
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
3. DO will hold until next DRP operation.

Clock Buffers and Networks

Table 59: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins Setup/Hold	0.11/ 0.00	0.13/ 0.00	0.16/ 0.00	0.13/ 0.00	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins Setup/Hold	0.11/ 0.00	0.13/ 0.00	0.16/ 0.00	0.13/ 0.00	ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O	0.07	0.08	0.10	0.10	ns
Maximum Frequency						
F_{MAX}	Global clock tree (BUFG)	800	750	700	667	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 60: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BIOCKO_O}	Clock to out delay from I to O	0.14	0.16	0.18	0.21	ns
Maximum Frequency						
F_{MAX}	I/O clock tree (BUFIO)	800	800	710	710	MHz

Table 61: **Regional Clock Switching Characteristics (BUFR)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BRCKO_O}	Clock to out delay from I to O	0.56	0.62	0.73	0.82	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.28	0.31	0.36	0.41	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.69	0.74	0.80	1.12	ns
Maximum Frequency						
F_{MAX}(1)	Regional clock tree (BUFR)	500	420	300	300	MHz

Notes:

1. The maximum input frequency to the BUFR is the BUFIO F_{MAX} frequency.

Table 62: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BHCKO_O}	BUFH delay from I to O	0.10	0.11	0.13	0.15	ns
$T_{BHCCK\_CE}/T_{BHCKC\_CE}$	CE pin Setup and Hold	0.04/ 0.04	0.04/ 0.04	0.05/ 0.05	0.04/ 0.04	ns
Maximum Frequency						
F_{MAX}	Horizontal clock buffer (BUFH)	800	750	700	667	MHz

MMCM Switching Characteristics

Table 63: **MMCM Specification**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F_{INMAX}	Maximum Input Clock Frequency	800	750	700	700	MHz
F_{INMIN}	Minimum Input Clock Frequency	10	10	10	10	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max				
F_{INDUTY}	Allowable Input Duty Cycle: 19—49 MHz	25/75				%
	Allowable Input Duty Cycle: 50—199 MHz	30/70				%
	Allowable Input Duty Cycle: 200—399 MHz	35/65				%
	Allowable Input Duty Cycle: 400—499 MHz	40/60				%
	Allowable Input Duty Cycle: >500 MHz	45/55				%
F_{MIN_PSCLK}	Minimum Dynamic Phase Shift Clock Frequency	0.01	0.01	0.01	0.01	MHz
F_{MAX_PSCLK}	Maximum Dynamic Phase Shift Clock Frequency	550	500	450	450	MHz
F_{VCOMIN}	Minimum MMCM VCO Frequency	600	600	600	600	MHz
F_{VCOMAX}	Maximum MMCM VCO Frequency	1600	1440	1200	1200	MHz
$F_{BANDWIDTH}$	Low MMCM Bandwidth at Typical(1)	1.00	1.00	1.00	1.00	MHz
	High MMCM Bandwidth at Typical(1)	4.00	4.00	4.00	4.00	MHz
$T_{STATPHAOFFSET}$	Static Phase Offset of the MMCM Outputs(2)	0.12	0.12	0.12	0.12	ns
$T_{OUTJITTER}$	MMCM Output Jitter(3)	Note 1				
$T_{OUTDUTY}$	MMCM Output Clock Duty Cycle Precision(4)	0.15	0.20	0.20	0.20	ns
$T_{LOCKMAX}$	MMCM Maximum Lock Time	100	100	100	100	µs
F_{OUTMAX}	MMCM Maximum Output Frequency	800	750	700	700	MHz
F_{OUTMIN}	MMCM Minimum Output Frequency(5)(6)	4.69	4.69	4.69	4.69	MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max				
$RST_{MINPULSE}$	Minimum Reset Pulse Width	1.5	1.5	1.5	1.5	ns
F_{PFDMAX}	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	550	500	450	450	MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	300	300	300	300	MHz
F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	10.00	10.00	10.00	10.00	MHz
$T_{FBDELAY}$	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle				
$T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$	Setup and Hold of Phase Shift Enable	1.04 0.00	1.04 0.00	1.04 0.00	1.04 0.00	ns
$T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$	Setup and Hold of Phase Shift Increment/Decrement	1.04 0.00	1.04 0.00	1.04 0.00	1.04 0.00	ns
$T_{MMCMCKO\_PSDONE}$	Phase Shift Clock-to-Out of PSDONE	0.32	0.34	0.38	0.38	ns

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Architecture Wizard.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When CASCADE4_OUT = TRUE, F_{OUTMIN} is 0.036 MHz.

Virtex-6 Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 64. Values are expressed in nanoseconds unless otherwise noted.

Table 64: **Global Clock Input to Output Delay Without MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *without* MMCM.							
T_{ICKOF}	Global Clock input and OUTFF *without* MMCM	XC6VLX75T	4.91	5.32	5.88	6.02	ns
		XC6VLX130T	4.89	5.33	6.00	6.13	ns
		XC6VLX195T	5.02	5.46	6.13	6.27	ns
		XC6VLX240T	5.02	5.46	6.13	6.27	ns
		XC6VLX365T	5.30	5.75	6.43	6.37	ns
		XC6VLX550T	N/A	6.02	6.72	6.60	ns
		XC6VLX760	N/A	6.26	6.97	6.87	ns
		XC6VSX315T	5.40	5.85	6.54	6.49	ns
		XC6VSX475T	N/A	6.01	6.71	6.61	ns
		XC6VHX250T	5.18	5.63	6.30	N/A	ns
		XC6VHX255T	5.20	5.66	6.34	N/A	ns
		XC6VHX380T	5.38	5.84	6.53	N/A	ns
		XC6VHX565T	N/A	5.85	6.56	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 65: **Global Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* MMCM.							
$T_{ICKOFMMCMGC}$	Global Clock Input and OUTFF *with* MMCM	XC6VLX75T	2.34	2.50	2.77	2.85	ns
		XC6VLX130T	2.35	2.51	2.78	2.87	ns
		XC6VLX195T	2.36	2.52	2.79	2.88	ns
		XC6VLX240T	2.36	2.52	2.79	2.88	ns
		XC6VLX365T	2.37	2.53	2.79	2.89	ns
		XC6VLX550T	N/A	2.55	2.82	2.93	ns
		XC6VLX760	N/A	2.54	2.82	2.92	ns
		XC6VSX315T	2.35	2.51	2.79	2.87	ns
		XC6VSX475T	N/A	2.43	2.70	2.79	ns
		XC6VHX250T	2.36	2.53	2.80	N/A	ns
		XC6VHX255T	2.46	2.63	2.91	N/A	ns
		XC6VHX380T	2.39	2.59	2.83	N/A	ns
		XC6VHX565T	N/A	2.54	2.81	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 66: **Clock-Capable Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS25 Clock-capable Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* MMCM.							
$T_{ICKOFMMCMCC}$	Clock-capable Clock Input and OUTFF *with* MMCM	XC6VLX75T	2.22	2.38	2.63	2.72	ns
		XC6VLX130T	2.24	2.39	2.65	2.74	ns
		XC6VLX195T	2.24	2.40	2.65	2.75	ns
		XC6VLX240T	2.24	2.40	2.65	2.75	ns
		XC6VLX365T	2.25	2.42	2.65	2.76	ns
		XC6VLX550T	N/A	2.43	2.68	2.80	ns
		XC6VLX760	N/A	2.42	2.69	2.79	ns
		XC6VSX315T	2.23	2.38	2.65	2.73	ns
		XC6VSX475T	N/A	2.30	2.57	2.66	ns
		XC6VHX250T	2.25	2.41	2.67	N/A	ns
		XC6VHX255T	2.35	2.51	2.78	N/A	ns
		XC6VHX380T	2.27	2.43	2.69	N/A	ns
		XC6VHX565T	N/A	2.41	2.68	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Virtex-6 Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 67. Values are expressed in nanoseconds unless otherwise noted.

Table 67: **Global Clock Input Setup and Hold Without MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T_{PSFD}/ T_{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock Input and IFF(2) without MMCM	XC6VLX75T	1.33/ 0.03	1.44/ 0.03	1.75/ 0.03	2.18/ –0.22	ns
		XC6VLX130T	1.31/ –0.08	1.54/ –0.08	1.88/ –0.08	2.31/ –0.12	ns
		XC6VLX195T	1.36/ –0.11	1.60/ –0.11	1.97/ –0.11	2.40/ –0.25	ns
		XC6VLX240T	1.36/ –0.11	1.60/ –0.11	1.97/ –0.11	2.40/ –0.25	ns
		XC6VLX365T	1.79/ –0.28	1.87/ –0.28	2.17/ –0.28	2.48/ –0.24	ns
		XC6VLX550T	N/A	2.22/ –0.12	2.36/ –0.12	2.77/ –0.26	ns
		XC6VLX760	N/A	2.19/ –0.24	2.35/ –0.24	2.71/ –0.21	ns
		XC6VSX315T	1.75/ –0.09	1.85/ –0.09	2.06/ –0.09	2.47/ –0.24	ns
		XC6VSX475T	N/A	2.14/ –0.14	2.31/ –0.14	2.71/ –0.30	ns
		XC6VHX250T	1.93/ –0.22	2.04/ –0.22	2.25/ –0.22	N/A	ns
		XC6VHX255T	1.81/ –0.33	2.11/ –0.33	2.56/ –0.33	N/A	ns
		XC6VHX380T	1.93/ –0.11	2.04/ –0.11	2.25/ –0.11	N/A	ns
		XC6VHX565T	N/A	2.38/ –0.12	2.54/ –0.12	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Table 68: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
$T_{PSMMCMGC}$/ $T_{PHMMCMGC}$	No Delay Global Clock Input and IFF(2) with MMCM	XC6VLX75T	1.45/ –0.18	1.57/ –0.18	1.72/ –0.18	1.78/ –0.08	ns
		XC6VLX130T	1.53/ –0.18	1.65/ –0.18	1.81/ –0.18	1.87/ –0.07	ns
		XC6VLX195T	1.54/ –0.17	1.66/ –0.17	1.82/ –0.17	1.87/ –0.08	ns
		XC6VLX240T	1.54/ –0.17	1.66/ –0.17	1.82/ –0.17	1.87/ –0.08	ns
		XC6VLX365T	1.55/ –0.18	1.67/ –0.18	1.83/ –0.18	1.87/ –0.07	ns
		XC6VLX550T	N/A	1.84/ –0.17	2.02/ –0.17	2.06/ –0.06	ns
		XC6VLX760	N/A	2.26/ –0.13	2.49/ –0.13	2.06/ –0.03	ns
		XC6VSX315T	1.56/ –0.18	1.68/ –0.18	1.84/ –0.18	1.89/ –0.08	ns
		XC6VSX475T	N/A	1.85/ –0.23	2.03/ –0.23	2.07/ –0.13	ns
		XC6VHX250T	1.52/ –0.17	1.64/ –0.17	1.80/ –0.17	N/A	ns
		XC6VHX255T	1.52/ –0.12	1.64/ –0.12	1.80/ –0.12	N/A	ns
		XC6VHX380T	1.68/ –0.16	1.81/ –0.16	1.99/ –0.16	N/A	ns
		XC6VHX565T	N/A	1.81/ –0.16	1.99/ –0.16	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 69: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Clock-capable Clock Input Signal for LVCMOS25 Standard.(1)							
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No Delay Clock-capable Clock Input and IFF(2) with MMCM	XC6VLX75T	1.56/ –0.25	1.69/ –0.25	1.86/ –0.25	1.91/ –0.15	ns
		XC6VLX130T	1.64/ –0.25	1.78/ –0.25	1.95/ –0.25	2.00/ –0.14	ns
		XC6VLX195T	1.65/ –0.24	1.79/ –0.24	1.96/ –0.24	2.01/ –0.15	ns
		XC6VLX240T	1.65/ –0.24	1.79/ –0.24	1.96/ –0.24	2.01/ –0.15	ns
		XC6VLX365T	1.66/ –0.25	1.79/ –0.25	1.97/ –0.25	2.02/ –0.15	ns
		XC6VLX550T	N/A	1.97/ –0.24	2.16/ –0.24	2.19/ –0.14	ns
		XC6VLX760	N/A	2.39/ –0.20	2.63/ –0.20	2.21/ –0.10	ns
		XC6VSX315T	1.67/ –0.25	1.80/ –0.25	1.98/ –0.25	2.03/ –0.16	ns
		XC6VSX475T	N/A	1.98/ –0.29	2.17/ –0.29	2.21/ –0.20	ns
		XC6VHX250T	1.63/ –0.24	1.76/ –0.24	1.94/ –0.24	N/A	ns
		XC6VHX255T	1.63/ –0.19	1.76/ –0.19	1.94/ –0.19	N/A	ns
		XC6VHX380T	1.80/ –0.23	1.94/ –0.23	2.13/ –0.23	N/A	ns
		XC6VHX565T	N/A	1.94/ –0.23	2.13/ –0.23	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-6 FPGA clock transmitter and receiver data-valid windows.

Table 70: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion(1)	All	0.12	0.12	0.12	0.12	ns
T_{CKSKEW}	Global Clock Tree Skew(2)	XC6VLX75T	0.15	0.16	0.18	0.17	ns
		XC6VLX130T	0.25	0.26	0.29	0.28	ns
		XC6VLX195T	0.26	0.27	0.31	0.30	ns
		XC6VLX240T	0.26	0.27	0.31	0.30	ns
		XC6VLX365T	0.28	0.29	0.31	0.31	ns
		XC6VLX550T	N/A	0.50	0.54	0.54	ns
		XC6VLX760	N/A	0.51	0.56	0.56	ns
		XC6VSX315T	0.27	0.28	0.32	0.30	ns
		XC6VSX475T	N/A	0.39	0.44	0.42	ns
		XC6VHX250T	0.25	0.26	0.29	N/A	ns
		XC6VHX255T	0.35	0.37	0.41	N/A	ns
		XC6VHX380T	0.45	0.47	0.52	N/A	ns
		XC6VHX565T	N/A	0.46	0.51	N/A	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.08	0.08	0.08	0.08	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.03	0.03	0.03	0.02	ns
$T_{BUFIOSKEW2}$	I/O clock tree skew across three clock regions	All	0.10	0.12	0.23	0.12	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	0.15	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 71: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XC6VLX75T	FF484	82	ps
			FF784	108	ps
		XC6VLX130T	FF484	78	ps
			FF784	126	ps
			FF1156	165	ps
		XC6VLX195T	FF784	128	ps
			FF1156	131	ps
		XC6VLX240T	FF784	146	ps
			FF1156	182	ps
			FF1759	187	ps
		XC6VLX365T	FF1156	137	ps
			FF1759	156	ps
		XC6VLX550T	FF1759	159	ps
			FF1760	202	ps
		XC6VLX760	FF1760	194	ps
		XC6VSX315T	FF1156	139	ps
			FF1759	162	ps
		XC6VSX475T	FF1156	131	ps
			FF1759	161	ps
		XC6VHX250T	FF1154	159	ps
		XC6VHX255T	FF1155		ps
			FF1923	220	ps
		XC6VHX380T	FF1154		ps
			FF1155	172	ps
			FF1923	227	ps
			FF1924	220	ps
		XC6VHX565T	FF1923		ps
			FF1924		ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Table 72: **Sample Window**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
T_{SAMP}	Sampling Error at Receiver Pins(1)	All	510	560	610	670	ps
T_{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO(2)	All	300	350	400	440	ps

Notes:

1. This parameter indicates the total sampling error of Virtex-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of Virtex-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IODELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 73: **Pin-to-Pin Setup/Hold and Clock-to-Out**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO						
T_{PSCS}/T_{PHCS}	Setup/Hold of I/O clock	–0.28 1.09	–0.28 1.16	–0.28 1.33	–0.18 1.79	ns
Pin-to-Pin Clock-to-Out Using BUFIO						
$T_{ICKOFCS}$	Clock-to-Out of I/O clock	4.22	4.59	5.22	5.63	ns

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
06/24/09	1.0	Initial Xilinx release.
07/16/09	1.1	Revised the maximum V_{CCAUX} and V_{IN} numbers in Table 2, page 2. Removed empty column from Table 3, page 2. Revised specifications on Table 20, page 11. Updated Table 38, page 20 and added notes 1 and 2. Revised T_{DLYCCO_RDY}, $T_{IDELAYCTRL\_RPW}$, and $T_{IDELAYPAT\_JIT}$ in Table 52, page 35. Updated Table 57, page 40 to more closely match the DSP48E1 speed specifications. Updated T_{TAPTCK}/T_{TCKTAP} in Table 58, page 43. Updated XC6VLX130T parameters in Table 67 through Table 69, page 52.
08/19/09	1.2	Added values for -1L voltages and speed grade in all pertinent tables. Added V_{FS} and notes to Table 1 and Table 2. Removed DV_{PPIN} from the example in Figure 2. Added networking applications to Table 41, page 23. Changed and added to the block RAM F_{MAX} section in Table 56, page 39 including removing Note 12. Changed F_{PFDMAX} values and corrected units for $T_{STATPHAOFFSET}$ and $T_{OUTDUTY}$ in Table 63, page 47. Updated Table 70, page 53.
09/16/09	2.0	Added Virtex-6 HXT devices to entire document including GTH Transceiver Specifications. Updated speed specifications as described in Switching Characteristics, includes changes in Table 50, Table 56, Table 57, and Table 65 through Table 69. Comprehensive changes to Table 14, Table 15, and Table 16. Added conditions to D_{VPPOUT} and revised description of T_{OSKEW} in Table 17. Removed V_{ISE} specification and note from Table 18. Added note 3 to Table 23. Updated note 3 in Table 24. Updated LVCMOS25 delays in Table 44. Updated specification for T_{IOTPHZ} in Table 45. Removed $T_{BUFHSKEW}$ from Table 70, page 53 and added values for $T_{BUFIOSKEW}$. Added values in Table 73.

Date	Version	Description of Revisions
01/18/10	2.1	Changed absolute maximum ratings for both V_{IN} and V_{TS} in Table 1. Added data to Table 3. Added data to Table 5. Updated SSTL15 in Table 7. Updated V_{OCM} and V_{OD} values in Table 8. Added eFUSE endurance Table 12. Added values to $V_{MGTREFCLK}$ and V_{IN} in Table 13, page 9. Added values and updated tables in the GTX Transceiver Specifications and GTH Transceiver Specifications sections. Added Table 27 and Figure 4. Revised parameters and values in Table 39. Updated Table 40, page 21. Added data to Table 41. Updated speed specification to v1.04 with appropriate changes to Table 42 and Table 43 including production release of the XC6VLX240T for -1 and -2 speed grades. Speed specification changes and numerous updates also made to Table 44, and Table 48 through Table 70. Added data to Table 72 and Table 73.
02/09/10	2.2	Revised description of C_{IN} in Table 3. Clarified values in Table 5. Fixed SDR LVDS unit error in Table 41.
04/12/10	2.3	Added note 3 and update value of *n* in Table 3. Clarified simultaneous power-down in Power-On Power Supply Requirements. Updated external reference junction temperatures in Table 40, Analog-to-Digital Specifications. Updated speed specification to v1.05 with appropriate changes to Table 42 and Table 43 including production release of the XC6VLX130T for -1 and -2 speed grades. Fixed note 4 in Table 47. Increased the -2 specification for $F_{IDELAYCTRL\_REF}$ and clarified units for $T_{IDELAYPAT\_JIT}$ in Table 52. Added note 1 to Table 61.
05/11/10	2.4	Updated F_{RXREC} in Table 22. Revised $F_{IDELAYCTRL\_REF}$ in Table 52. Removed $T_{RCKO\_PARITY\_ECC}$: Clock CLK to ECCPARITY in standard ECC mode row in Table 56. Added XC6VLX130T values to Table 71.
05/26/10	2.5	Added XC6VLX195T data to Table 5. Updated values in Table 22 including adding note 2 and note 3. Updated speed specification to v1.06 with appropriate changes to Table 42 and Table 43 including production release of the XC6VLX195T for -1 and -2 speed grades. Added XC6VLX195T values to Table 71.
07/16/10	2.6	Changed Table 42 and Table 43 to production status on the -3 speed grade XC6VLX130T, XC6VLX195T, and XC6VLX240T devices. Added XC6VHX250Tdata to Table 4 and Table 71. Added Note 6 to Table 63.
07/23/10	2.7	Changed Table 42 and Table 43 to production status on the XC6VLX75T, XC6VLX365T, XC6VLX550T, XC6VLX760, XC6VSX315T, and XC6VSX475T devices using ISE 12.2 software with speed specification v1.08. Updated $V_{CMOUTDC}$ equation to MGTAVTT – D_{VPPOUT}/4 in Table 17. Updated some -3, -2, -1 specifications in Table 64 through Table 71. Added and updated -1L specifications to Table 41 and for most switching characteristics tables.
07/30/10	2.8	Changed Table 42 and Table 43 to production status on the -1L speed grade for the XC6VLX130T, XC6VLX195T, XC6VLX240T, XC6VLX365T, and XC6VLX550T devices using ISE 12.2 software with current speed specifications. Also updated the speed specifications for XC6VLX75T, XC6VLX550T, and XC6VSX315T. Updated V_{CCINT} specifications for -1L speed grade industrial temperature range devices in Table 2.
09/20/10	2.9	In Table 32, changed $F_{GPLLMAX}$ specification in -3 column from 5.951 to 5.591. In Table 40, changed F_{MAX} for the DCLK from 250 MHz to 80 MHz.
10/18/10	2.10	The specification change in version 2.9, Table 40 is described in XCN10032, *Virtex-6 FPGA: GTX Transceiver User Guide, Family Data Sheet (SYSMON DCLK), and JTAG ID Changes* In this version (2.10), -1L(I) data is added to Table 4 and clarified in Note 2. Changed Table 42 and Table 43 to production status on the -1L speed grade XC6VLX75T, XC6VLX760, XC6VSX315T, and XC6VSX475T devices using ISE 12.3 software with current speed specifications. Revised the XC6VLX760 -1L speed specification for $T_{PHMMCMGC}$ in Table 68 and $T_{PHMMCMCC}$ in Table 69.

Notice of Disclaimer