NEC

NEC Electronics Inc.

μPD75P108
4-BIT, SINGLE-CHIP CMOS MICROCOMPUTER WITH ON-CHIP EPROM

PRELIMINARY INFORMATION

Description

The μPD75P108 is a high-performance, single-chip CMOS microcomputer that incorporates a CPU, ROM, RAM, I/O ports, vector interrupt functions, serial interface, and timer/event counters.

The device is functionally equivalent and pin-compatible with the μPD75104/μPD75106/μPD75108. The EPROM in the μPD75P108 allows you to evaluate your program before placing the mask order. An OTP ROM version is available for small production runs.

Features

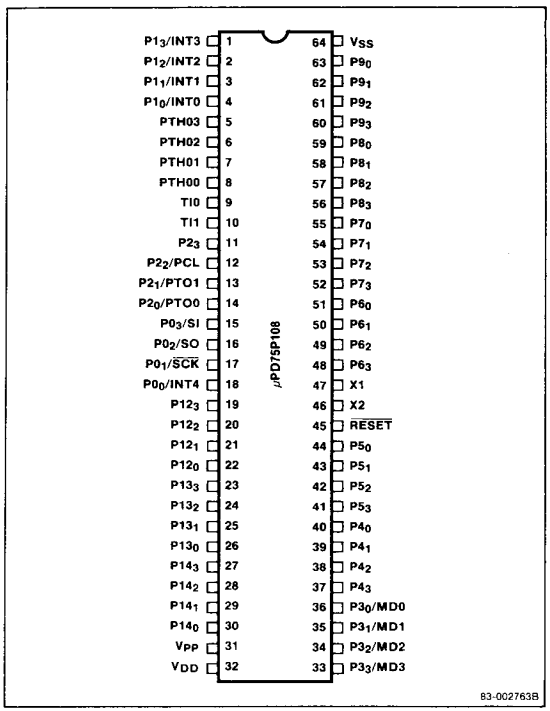
- ☐ 46 instructions
  - — Bit manipulation instructions
  - — 8-bit data transfer, comparison, and increment/decrement instructions
  - — 1-byte relative branch instructions
  - — GETI instruction that realizes 2-or 3-byte instructions in 1-byte units
- ☐ Instruction cycles
  - — High-speed cycle: 0.95 μs/4.19 MHz, V_{DD} = 5 V
  - — Low-voltage cycle: 1.91 μs/4.19 MHz, 15.3 μs/4.19 MHz
- ☐ Program memory (EPROM): 8192 x 8 bits
- ☐ Data memory (RAM): 512 x 4 bits
- ☐ Bit manipulation memory (bit-sequential buffer): 16 bits
- ☐ Four banks of 8 x 4-bit general-purpose registers
- ☐ Accumulators
  - — Bit accumulator (CY)
  - — 4-Bit accumulator (A)
  - — 8-Bit accumulator (XA)
- ☐ 58 I/O lines
  - — High-current output ports that can directly drive LEDs (total of 200 mA for 32 pins)
  - — 12 N-channel open-drain outputs with 12 V maximum
  - — Four programmable comparator threshold inputs
  - — Two external event inputs
- ☐ Vectored interrupt function capable of multiple interrupts
  - — Three external vectored interrupts
  - — Two external test inputs
  - — Four internal vectored interrupts
- ☐ Two 8-bit timer/event counters
- ☐ 8-bit serial interface
  - — Data transfer can start with LSB or MSB
  - — Two transfer modes (transmit/receive and receive-only)
- ☐ Power-on reset circuit
- ☐ Crystal or ceramic oscillator
- ☐ Standby modes (STOP/HALT)
- ☐ CMOS technology
- ☐ Low power consumption

Ordering Information

Part Number	Package Type	ROM (8K x 8)
μPD75P108DW	64-pin shrink cerdip with window	EPROM
μPD75P108CW	64-pin plastic shrink DIP	OTP ROM
μPD75P108G-1B	64-pin plastic miniflat	OTP ROM

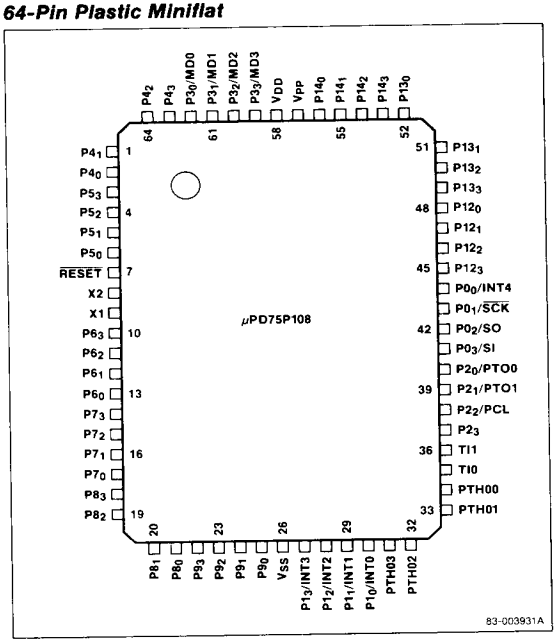
Pin Configurations

64-Pin Ceramic Shrink DIP or Shrink Cerdip with Window



Pin Configurations (cont)

64-Pin Plastic Miniflat



Pin Identification

Symbol	Function
$P1_3$/INT3 $P1_2$/INT2 $P1_1$/INT1 $P1_0$/INT0	4-bit input port 1/Edge-triggered vectored interrupts
PTH03-PTH00	Programmable threshold comparator analog input port
TI0, TI1	External event input for timer/event counter
$P2_3$, $P2_2$/PCL $P2_1$/PTO1 $P2_0$/PTO0	4-bit I/O port 2/Clock output terminal/Timer/event counter output pins
$P0_3$/SI $P0_2$/SO $P0_1$/SCK $P0_0$/INT4	4-bit input port 0/Serial interface/Edge-triggered vectored interrupt
$P12_3$-$P12_0$	4-bit I/O port 12
$P13_3$-$P13_0$	4-bit I/O port 13
$P14_3$-$P14_0$	4-bit I/O port 14
V_{PP}	EPROM programming power supply
V_{DD}	Positive power supply
$P3_3$/MD3 $P3_2$/MD2 $P3_1$/MD1 $P3_0$/MD0	Programmable 4-bit I/O port 3/EPROM function mode selection inputs
$P4_3$-$P4_0$	4-bit I/O port 4
$P5_3$-$P5_0$	4-bit I/O port 5
$\overline{RESET}$	Reset input
X2, X1	Ceramic or crystal system clock oscillator
$P6_3$-$P6_0$	Programmable 4-bit I/O port 6
$P7_3$-$P7_0$	4-bit I/O port 7
$P8_3$-$P8_0$	4-bit I/O port 8
$P9_3$-$P9_0$	4-bit I/O port 9
V_{SS}	Ground

Pin Functions

$P0_0$/INT_4, $P0_1$/$\overline{SCK}$, $P0_2$/SO, $P0_3$/SI [Port 0, Interrupt, Serial Clock, Serial Interface]

This port can be configured as a 4-bit parallel input port or as the serial I/O interface under control of the serial mode select register. The serial input SI, serial output SO, and the serial clock $\overline{SCK}$ make up the serial I/O interface. INT4 is an edge-triggered vectored interrupt triggered by a rising or falling edge. The port is in the input state at reset.

$P1_3$/INT3, $P1_2$/INT2, $P1_1$/INT1, $P1_0$/INT0 [Port 1, Edge-Triggered Interrupts]

4-bit input port 1/interrupts. INT0 and INT1 are edge-triggered vectored interrupts selected by a rising or falling edge. INT2 and INT3 are triggered by a rising edge only. The port and the interrupts are in the input state at reset.

$P2_3$, $P2_2$/PCL, $P2_1$/PTO1, $P2_0$/PTO0 [Port 2, Clock Output, Timer/Event Counter Output]

Port 2 is a 4-bit I/O port for directly driving LEDs. PTO1 and PTO0 are the timer/event counter output pins. PCL is the clock output pin. These pins are in the input state at reset.

$P3_3$/MD3, $P3_2$/MD2, $P3_1$/MD1, $P3_0$/MD0 [Port 3, EPROM Function Mode Inputs]

Programmable 4-bit I/O port for directly driving LEDs with bit-level I/O selection. MD0-MD3 select the EPROM operating mode. The port is in the input state at reset.

$P4_3$-$P4_0$ [Port 4]

4-bit I/O port for directly driving LEDs. The port is in the input state at reset and has 8-bit I/O capability when paired with port 5.

Pin Functions (cont)

$P5_3$-$P5_0$ [Port 5]

4-bit I/O port for directly driving LEDs. The port is in the input state at reset and has 8-bit I/O capability when paired with port 4.

$P6_3$-$P6_0$ [Port 6]

Programmable 4-bit I/O port for directly driving LEDs with bit-level I/O selection. The port is in the input state at reset and has 8-bit I/O capability when paired with port 7.

$P7_3$-$P7_0$ [Port 7]

4-bit I/O port for directly driving LEDs. The port is in the input state at reset and has 8-bit I/O capability when paired with port 6.

$P8_3$-$P8_0$ [Port 8]

4-bit I/O port for directly driving LEDs. The port is in the input state at reset and has 8-bit I/O capability when paired with port 9.

$P9_3$-$P9_0$ [Port 9]

4-bit I/O port for directly driving LEDs. The port is in the input state at reset and has 8-bit I/O capability when paired with port 8.

$P12_3$-$P12_0$ [Port 12]

4-bit I/O port, N-channel, open-drain (12 V max). The port is in the high-impedance state at reset and has 8-bit I/O capability when paired with port 13.

$P13_3$-$P13_0$ [Port 13]

4-bit I/O port, N-channel, open-drain (12 V max). The port is in the high-impedance state at reset and has 8-bit I/O capability when paired with port 12.

$P14_3$-$P14_0$ [Port 14]

4-bit I/O port, N-channel, open-drain (12 V max). The port is in the high-impedance state at reset.

PTH03-PTH00 [Threshold Detector Analog Input Port]

Threshold detector analog input port.

TI0, TI1 [Timer/Event Counter Input]

External event input for the timer/event counter. These two pins are also an edge-triggered vectored interrupt and a 1-bit input port.

$\overline{\text{RESET}}$ [Reset]

System reset input pin (active low).

X2, X1 [System Clock I/O]

These pins are the system clock I/O. The clock may be ceramic or crystal.

V_{DD} [Power Supply]

Positive power supply.

V_{PP} [EPROM Programming Power Supply]

During normal operation, connect to V_{DD}. Connect to +21 V for EPROM programming.

V_{SS} [Ground]

System ground.

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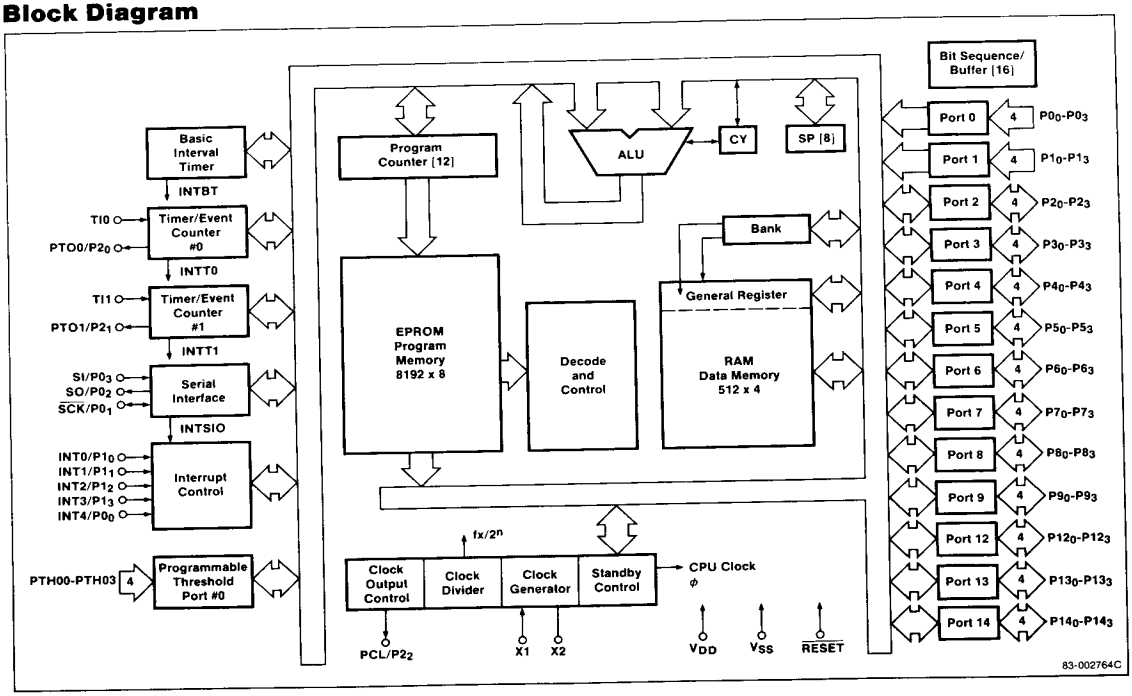
Block Diagram



μPD75000 Series

Table 1 compares the features of similar products in the μPD75000 series.

Table 1. Product Comparison

Item	μPD75P108	μPD75104	μPD75106	μPD75108
Program memory	EPROM 0000-1FFFH	Mask ROM 0000-0FFFH	Mask ROM 0000-177FH	Mask ROM 0000-1FFFH
Data memory	512 x 4-bit Bank 0: 256 Bank 1: 256	320 x 4-bit Bank 0: 256 Bank 1: 64	320 x 4-bit Bank 0: 256 Bank 1: 64	512 x 4-bit Bank 0: 256 Bank 1: 256
Instruction set	Set P108	Set P108 minus BR!addr (3-byte instr.)	Set P108	Set P108
Ports 12-14 pull-up resistor	Not offered	Mask option	Mask option	Mask option
Power-on reset	Integrated	Mask option	Mask option	Mask option
Power-on flag	Integrated	Mask option	Mask option	Mask option
Operating voltage	5 V ±10%	2.5 to 6.0 V	2.5 to 6.0 V	2.5 to 6.0 V
Pin 31	V_{PP}	NC	NC	NC
Packaging	64-pin ceramic shrink DIP or plastic miniflat	64-pin plastic miniflat or shrink DIP	64-pin plastic miniflat or shrink DIP	64-pin plastic miniflat or shrink DIP

EPROM Programming

The internal 8K-byte EPROM is programmed via the pins and functions listed in table 2. Refer to the flowchart, figure 1.

The V_{PP} and V_{DD} pins must be held at 5 V for at least 10 μs upon power-up and before the programming voltages of 21 V to V_{PP} and 6 V to V_{DD} are applied.

Mode pins MD_0-MD_3 control the programming steps as shown in table 3. Address inputs are not used during programming. The program memory address is first cleared via the mode pins, then incremented by applying four clock pulses to the X1 input.

Table 2. EPROM Access

Pin	Function
V_{PP}	Programming voltage. Connect to 21 V when programming EPROM.
X1, X2	Address increment clock input. X2 inputs the inverse of X1.
MD_0-MD_3	Mode selection
$P4_0$-$P4_3$	8-bit data bus connection, low
$P5_0$-$P5_3$	8-bit data bus connection, high
V_{DD}	Connect to 6 V during programming.

Table 3. EPROM Mode Selection

V_{PP} = 21 V, V_{DD} = 6.0 V

MD0	MD1	MD2	MD3	Operating Mode
H	L	H	L	Program memory address clear
L	H	H	H	Program memory write
L	L	H	H	Program verify
H	X	H	H	Program inhibit

I/O Port Interfaces

Figure 2 shows the internal circuit configurations at the I/O ports.

Figure 1. EPROM Programming Flowchart

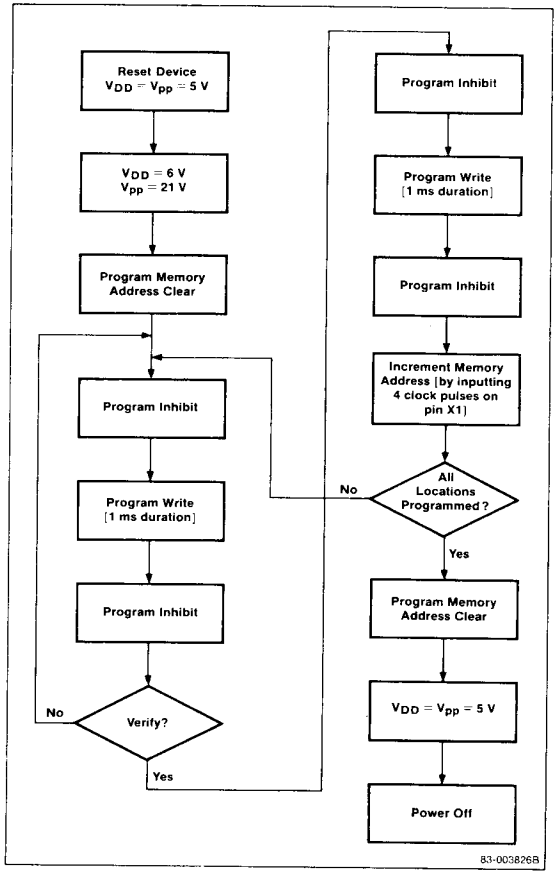


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Figure 2. Interface at Input/Output Ports