BLF7G10L-250; BLF7G10LS-250

Power LDMOS transistor

Rev. 5 — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

250 W LDMOS power transistor for base station applications at frequencies from 869 MHz to 960 MHz.

Table 1. Typical performance

Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7.5 dB at 0.01 % probability on CCDF per carrier; carrier spacing = 5 MHz. Typical RF performance at T_{case} = 25 °C.

Test signal	f (MHz)	I_{Dq} (mA)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	ACPR (dBc)
2-carrier W-CDMA	869 to 894 [1]	1800	30	60	19.5	27.4	−35.6
2-carrier W-CDMA	920 to 960 [2]	1800	30	60	19.5	30.5	−34

[1] In a common source class-AB application test circuit.

[2] In a common source class-AB production test circuit.

1.2 Features and benefits

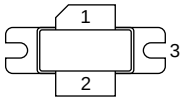
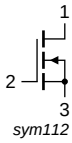
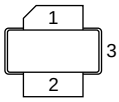
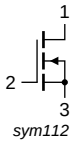
- Excellent ruggedness
- High efficiency
- Low R_{th} providing excellent thermal stability
- Designed for broadband operation (869 MHz to 960 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use (input and output)
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi carrier applications in the 869 MHz to 960 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
BLF7G10L-250 (SOT502A)				
1	drain			
2	gate			
3	source	[1]		
BLF7G10LS-250 (SOT502B)				
1	drain			
2	gate			
3	source	[1]		

[1] Connected to flange

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF7G10L-250	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A
BLF7G10LS-250	-	earless flanged ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 60 W (CW); V_{DS} = 30 V; I_{Dq} = 1800 mA	0.38	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 3.3 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 330 mA	1.50	1.9	2.30	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	5	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	56	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	0.5	mA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 11.55 A	-	22	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 11.55 A	-	57	-	mΩ

Table 7. RF characteristics

Test signal: 2-carrier W-CDMA; PAR = 7.5 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH; f_1 = 920 MHz; f_2 = 925 MHz; f_3 = 955 MHz; f_4 = 960 MHz; RF performance at V_{DS} = 30 V; I_{Dq} = 1800 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 60 W	18.5	19.5	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 60 W	-	−15.5	−10	dB
η_D	drain efficiency	$P_{L(AV)}$ = 60 W	27	30.5	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 60 W	-	−34	−31	dBc

7. Test information

7.1 Ruggedness in class-AB operation

The BLF7G10L-250 and BLF7G10LS-250 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 30 V; I_{Dq} = 1800 mA; P_L = 200 W (CW); f = 920 MHz to 960 MHz.

7.2 Impedance information

Table 8. Typical impedance information

I_{Dq} = 1800 mA; main transistor V_{DS} = 30 V.
Z_S and Z_L defined in Figure 1.

f (MHz)	Z_S (Ω)	Z_L (Ω)
925	3.1 – j3.3	1.0 – j1.7
942	3.2 – j3.3	1.0 – j1.6
960	3.4 – j3.5	0.9 – j1.4