SBAS254D – SEPTEMBER 2002 – REVISED MARCH 2004

Quad Channel, Low Power, 16-Bit, Serial Input DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **POWER SUPPLY: +2.7V to +5.5V**
- ***micro*POWER OPERATION: 950μA at 5V**
- **16-BIT MONOTONIC OVER TEMPERATURE**
- **SETTLING TIME: 10μs to ±0.003% FSR**
- **ULTRA-LOW AC CROSSTALK: –100dB typ**
- **POWER-ON RESET TO ZERO-SCALE**
- **ON-CHIP OUTPUT BUFFER AMPLIFIER WITH RAIL-TO-RAIL OPERATION**
- **DOUBLE BUFFERED INPUT ARCHITECTURE**
- **SIMULTANEOUS OR SEQUENTIAL OUTPUT UPDATE AND POWER-DOWN**
- **16 CHANNEL BROADCAST CAPABILITY**
- **SCHMITT-TRIGGERED INPUTS**
- **TSSOP-16 PACKAGE**

APPLICATIONS

- **PORTABLE INSTRUMENTATION**
- **CLOSED-LOOP SERVO-CONTROL**
- **PROCESS CONTROL**
- **DATA ACQUISITION SYSTEMS**
- **PROGRAMMABLE ATTENUATION**
- **PC PERIPHERALS**

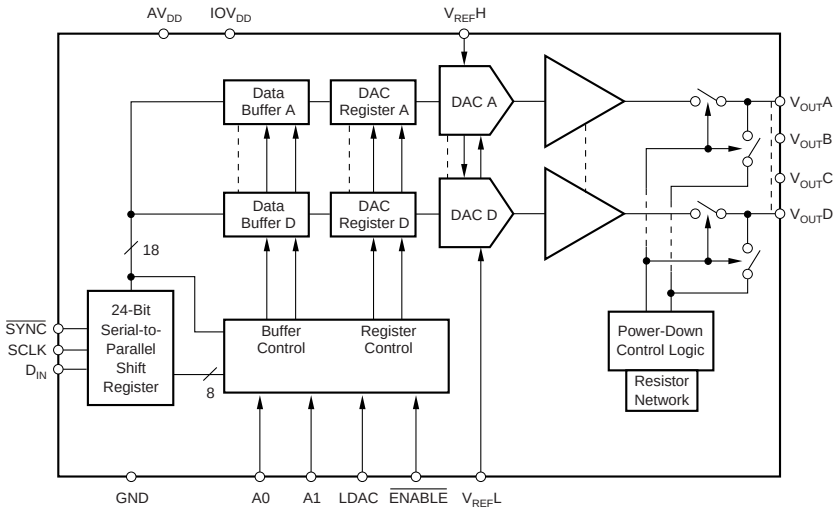
DESCRIPTION

The DAC8534 is a quad channel, 16-bit Digital-to-Analog Converter (DAC) offering low-power operation and a flexible serial host interface. Each on-chip precision output amplifier allows rail-to-rail output swing to be achieved over the supply range of 2.7V to 5.5V. The device supports a standard 3-wire serial interface capable of operating with input data clock frequencies up to 30MHz for IOV_{DD} = 5V.

The DAC8534 requires an external reference voltage to set the output range of each DAC channel. Also incorporated into the device is a power-on reset circuit which ensures that the DAC outputs power up at zero-scale and remain there until a valid write takes place. The DAC8534 provides a per channel power-down feature, accessed over the serial interface, that reduces the current consumption to 200nA per channel at 5V.

The low-power consumption of this device in normal operation makes it ideally suited to portable battery-operated equipment and other low-power applications. The power consumption is 5mW at 5V, reducing to 4μW in power-down mode.

The DAC8534 is available in a TSSOP-16 package with a specified operating temperature range of –40°C to +105°C.



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ABSOLUTE MAXIMUM RATINGS(1)

AV_{DD} to GND	–0.3V to +6V
Digital Input Voltage to GND	–0.3V to +AV_{DD} + 0.3V
V_{OUT}A to V_{OUT}D to GND	–0.3V to + AV_{DD} + 0.3V
Operating Temperature Range	–40°C to +105°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature Range (T_J max)	+150°C
Power Dissipation	(T_J max – T_A)/θ_{JA}
θ_{JA} Thermal Impedance	118°C/W
θ_{JC} Thermal Impedance	29°C/W
Lead Temperature, Soldering:	
Vapor Phase (60s)	+215°C
Infrared (15s)	+220°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFICATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8534	TSSOP-16	PW	–40°C to +105°C	D8534I	DAC8534IPW	Tube, 90
"	"	"	"	"	DAC8534IPWR	Tape and Reel, 2000

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

AV_{DD} = +2.7V to +5.5V, –40°C to +105°C, unless otherwise specified.

PARAMETER	CONDITIONS	DAC8534 MIN	DAC8534 TYP	DAC8534 MAX	UNITS
STATIC PERFORMANCE(1)					
Resolution		16			Bits
Relative Accuracy				±0.0987	% of FSR
Differential Nonlinearity	16-Bit Monotonic		0.25	±1	LSB
Zero-Scale Error			+5	+20	mV
Zero-Scale Error Drift			±7		µV/°C
Full-Scale Error			–0.15	–1.0	% of FSR
Gain Error				±1.0	% of FSR
Gain Temperature Coefficient			±3		ppm of FSR/°C
Channel-to-Channel Matching	R_L = 2kΩ, C_L = 200pF		8		mV
PSRR			0.75		mV/V
OUTPUT CHARACTERISTICS(2)					
Output Voltage Range		0		V_{REF}H	V
Output Voltage Settling Time	To ±0.003% FSR		8	10	µs
	0200_H to $FD00_H$				
	R_L = 2kΩ; 0pF < C_L < 200pF				
	R_L = 2kΩ; C_L = 500pF		12		µs
Slew Rate			1		V/µs
Capacitive Load Stability	R_L = ∞		470		pF
	R_L = 2kΩ		1000		pF
Code Change Glitch Impulse	1LSB Change Around Major Carry		20		nV-s
Digital Feedthrough			0.5		nV-s
DC Crosstalk			0.25		LSB
AC Crosstalk	1kHz sine Wave		–100	–96	dB
DC Output Impedance			1		Ω
Short-Circuit Current	AV_{DD} = +5V		50		mA
	AV_{DD} = +3V		20		mA
Power-Up Time	Coming Out of Power-Down Mode				
	AV_{DD} = +5V		2.5		µs
	Coming Out of Power-Down Mode				
	AV_{DD} = +3V		5		µs
AC PERFORMANCE	BW = 20kHz, AV_{DD} = 5V				
SNR (1st 19 Harmonics Removed)	F_{OUT} = 1kHz		94		dB
THD			67		dB
SFDR			69		dB
SINAD			65		dB

NOTES: (1) Linearity calculated using a reduced code range of 485 to 64714; output unloaded. (2) Ensured by design and characterization, not production tested.

ELECTRICAL CHARACTERISTICS (Cont.)

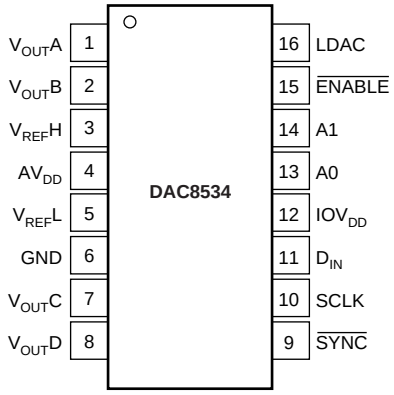
AV_{DD} = +2.7V to +5.5V, –40°C to +105°C, unless otherwise specified.

PARAMETER	CONDITIONS	DAC8534 MIN	DAC8534 TYP	DAC8534 MAX	UNITS
REFERENCE INPUT					
Reference Current	V_{REF} = AV_{DD} = +5V		135	180	µA
	V_{REF} = AV_{DD} = +3V		80	120	µA
Reference Input Range		0		AV_{DD}	V
Reference Input Impedance			37		kΩ
LOGIC INPUTS (2)					
Input Current				±1	µA
V_{IN}L, Input LOW Voltage	IOV_{DD} = +5V			0.8	V
V_{IN}L, Input LOW Voltage	IOV_{DD} = +3V			0.6	V
V_{IN}H, Input HIGH Voltage	IOV_{DD} = +5V	2.4			V
V_{IN}H, Input HIGH Voltage	IOV_{DD} = +3V	2.1			V
Pin Capacitance				3	pF
POWER REQUIREMENTS					
AV_{DD}		2.7		5.5	V
IOV_{DD}		2.7		5.5	V
AI_{DD} (normal mode)	DAC Active and Excluding Load Current				
IOI_{DD}			10	20	µA
AI_{DD} = +3.6V to +5.5V	V_{IH} = IOV_{DD} and V_{IL} = GND		0.95	1.6	mA
AI_{DD} = +2.7V to +3.6V	V_{IH} = IOV_{DD} and V_{IL} = GND		0.9	1.5	mA
AI_{DD} (all power-down modes)					
AI_{DD} = +3.6V to +5.5V	V_{IH} = IOV_{DD} and V_{IL} = GND		0.8	1	µA
AI_{DD} = +2.7V to +3.6V	V_{IH} = IOV_{DD} and V_{IL} = GND		0.05	1	µA
POWER EFFICIENCY					
I_{OUT}/I_{DD}	I_{LOAD} = 2mA, AV_{DD} = +5V		89		%
TEMPERATURE RANGE					
Specified Performance		–40		+105	°C

NOTES: (1) Linearity calculated using a reduced code range of 485 to 64714; output unloaded. (2) Ensured by design and characterization, not production tested.

PIN CONFIGURATION

Top View **TSSOP**



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	V_{OUT}A	Analog output voltage from DAC A.
2	V_{OUT}B	Analog output voltage from DAC B.
2	V_{REF}H	Positive reference voltage input.
4	AV_{DD}	Power supply input, +2.7V to +5.5V.
5	V_{REF}L	Negative reference voltage input.
6	GND	Ground reference point for all circuitry on the part.
7	V_{OUT}C	Analog output voltage from DAC C.
8	V_{OUT}D	Analog output voltage from DAC D.
9	$\overline{SYNC}$	Level-triggered control input (active LOW). This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes LOW, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 24th clock (unless $\overline{SYNC}$ is taken HIGH before this edge in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC8534).
10	SCLK	Serial Clock Input. Data can be transferred at rates up to 30MHz.
11	D_{IN}	Serial Data Input. Data is clocked into the 24-bit input shift register on each falling edge of the serial clock input.
12	IOV_{DD}	Digital Input-Output Power Supply
13	A0	Address 0 — sets device address, see Table II.
14	A1	Address 1 — sets device address, see Table II.
15	$\overline{ENABLE}$	Active LOW, $\overline{ENABLE}$ LOW connects the SPI interface to the serial port.
16	LDAC	Load DACs, rising edge triggered loads all DAC registers.

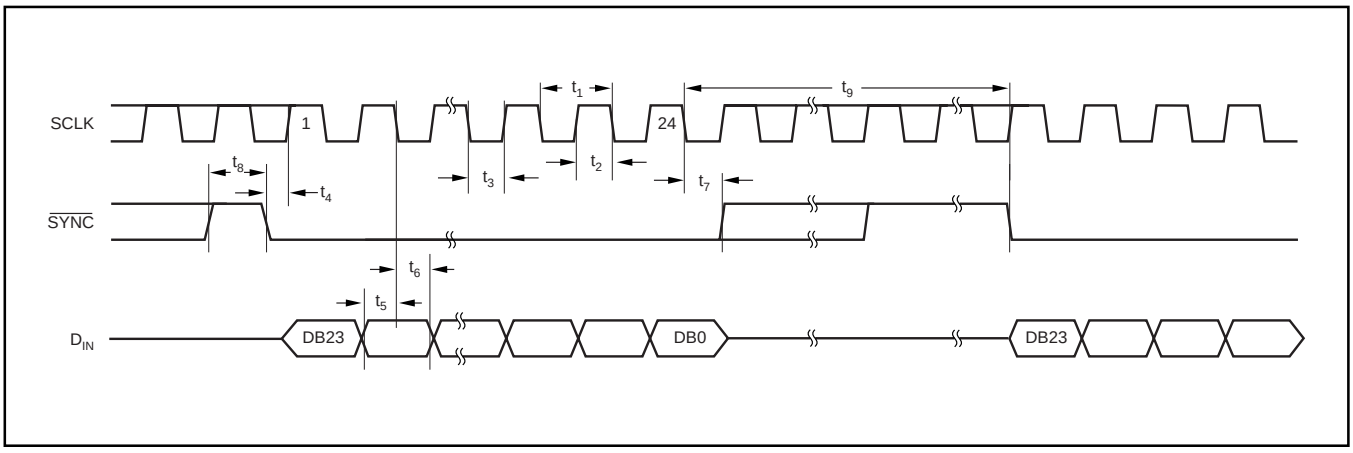
TIMING CHARACTERISTICS[1, 2]

AV_{DD} = +2.7V to +5.5V; all specifications –40°C to +105°C unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	DAC8534			UNITS
			MIN	TYP	MAX	
t_1[3]	SCLK Cycle Time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V IOV_{DD} = AV_{DD} = 3.6V to 5.5V	50 33			ns ns
t_2	SCLK HIGH Time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V IOV_{DD} = AV_{DD} = 3.6V to 5.5V	26 15			ns ns
t_3	SCLK LOW Time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V IOV_{DD} = AV_{DD} = 3.6V to 5.5V	22.5 13			ns ns
t_4	$\overline{SYNC}$ Falling Edge to SCLK Rising Edge Setup Time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V IOV_{DD} = AV_{DD} = 3.6V to 5.5V	0 0			ns ns
t_5	Data Setup Time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V IOV_{DD} = AV_{DD} = 3.6V to 5.5V	5 5			ns ns
t_6	Data Hold Time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V IOV_{DD} = AV_{DD} = 3.6V to 5.5V	4.5 4.5			ns ns
t_7	24th SCLK Falling Edge to $\overline{SYNC}$ Rising Edge	IOV_{DD} = AV_{DD} = 2.7V to 3.6V IOV_{DD} = AV_{DD} = 3.6V to 5.5V	0 0			ns ns
t_8	Minimum $\overline{SYNC}$ HIGH Time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V IOV_{DD} = AV_{DD} = 3.6V to 5.5V	50 33			ns ns
t_9	24th SCLK Falling Edge to $\overline{SYNC}$ Falling Edge	IOV_{DD} = AV_{DD} = 2.7V to 5.5V	130			ns

NOTES: (1) All input signals are specified with t_R = t_F = 3ns (10% to 90% of AV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. (2) See Serial Write Operation timing diagram, below. (3) Maximum SCLK frequency is 30MHz at IOV_{DD} = AV_{DD} = +3.6V to +5.5V and 20MHz at IOV_{DD} = AV_{DD} = +2.7V to +3.6V.

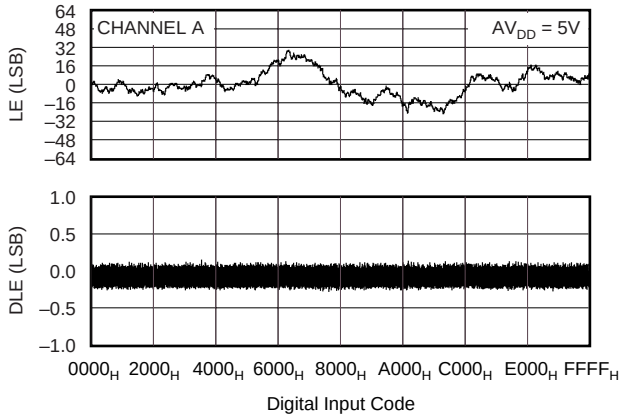
SERIAL WRITE OPERATION



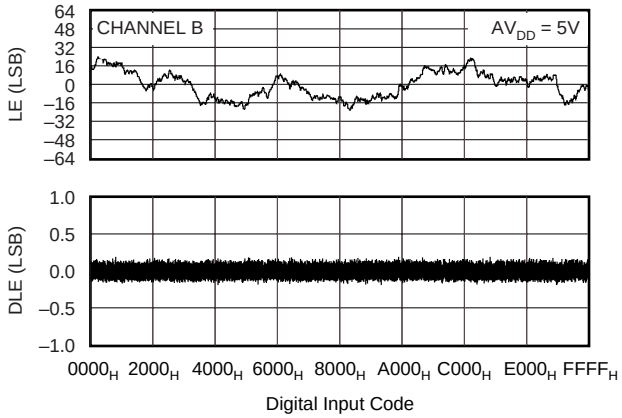
TYPICAL CHARACTERISTICS

At T_A = +25°C, unless otherwise noted.

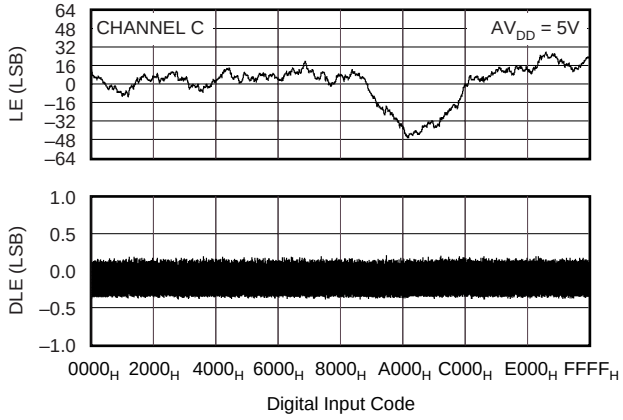
LINEARITY ERROR AND DIFFERENTIAL
LINEARITY ERROR vs DIGITAL INPUT CODE



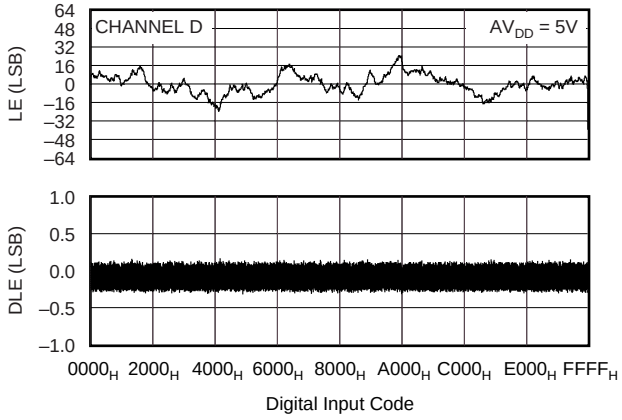
LINEARITY ERROR AND DIFFERENTIAL
LINEARITY ERROR vs DIGITAL INPUT CODE



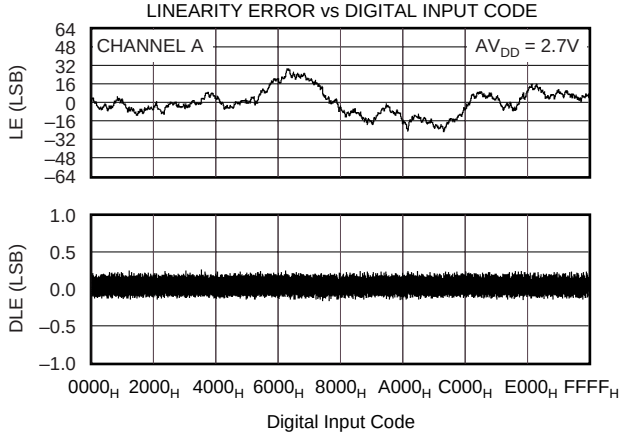
LINEARITY ERROR AND DIFFERENTIAL
LINEARITY ERROR vs DIGITAL INPUT CODE



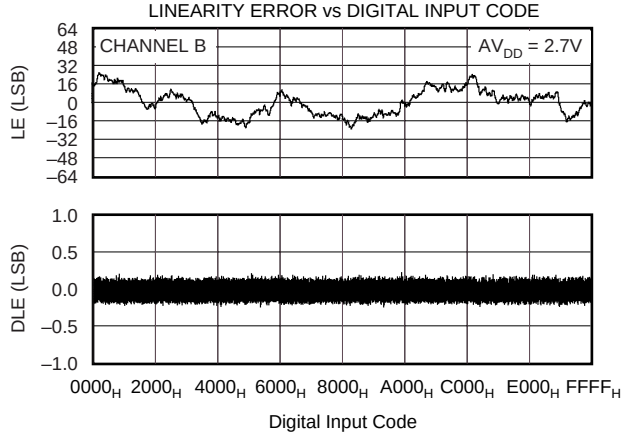
LINEARITY ERROR AND DIFFERENTIAL
LINEARITY ERROR vs DIGITAL INPUT CODE



LINEARITY ERROR AND DIFFERENTIAL
LINEARITY ERROR vs DIGITAL INPUT CODE



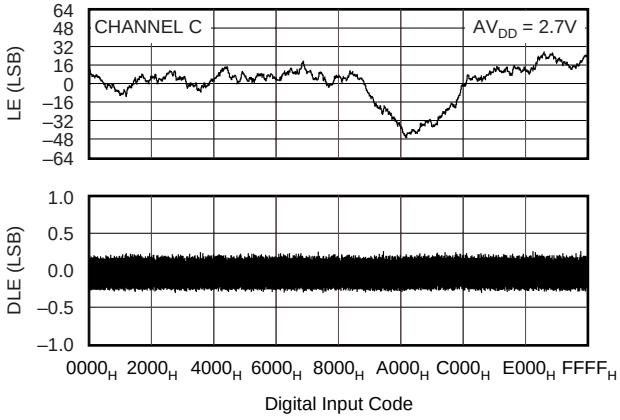
LINEARITY ERROR AND DIFFERENTIAL
LINEARITY ERROR vs DIGITAL INPUT CODE



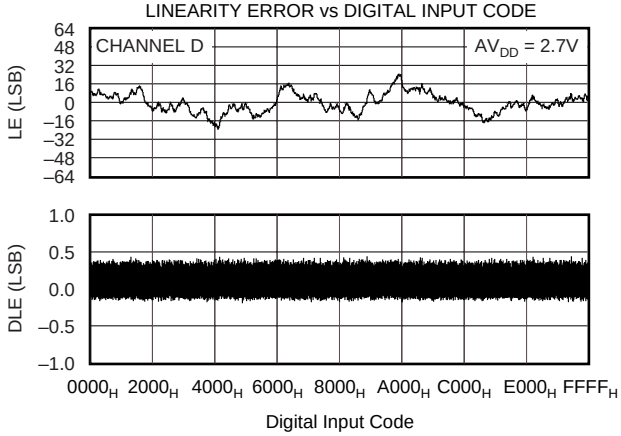
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, unless otherwise noted.

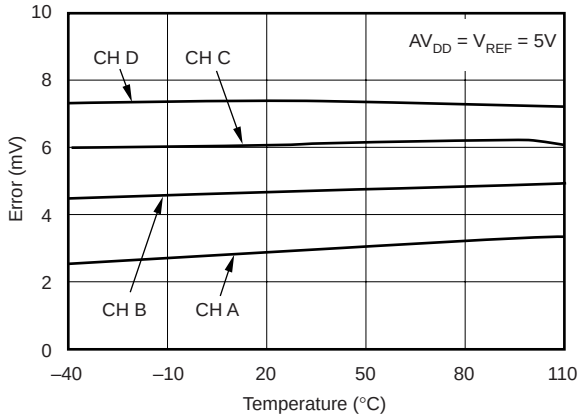
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE



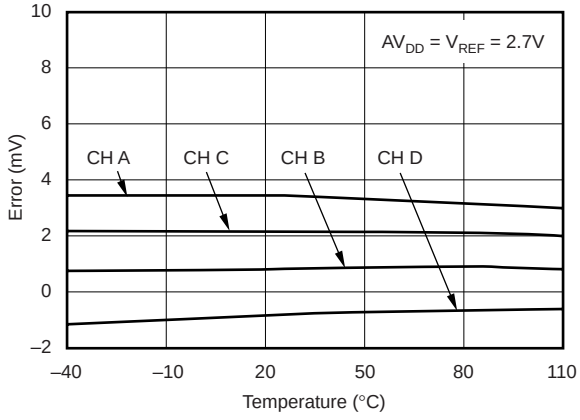
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE



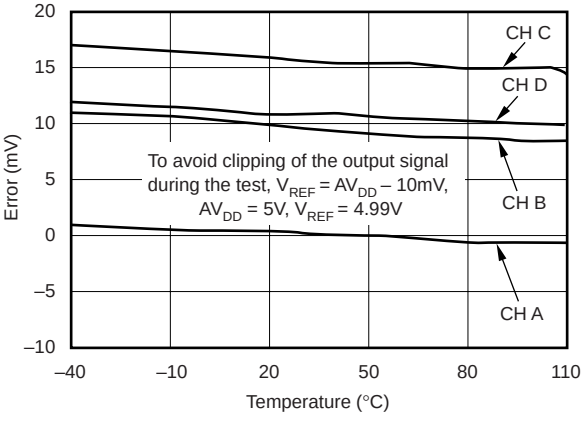
ZERO-SCALE ERROR vs TEMPERATURE



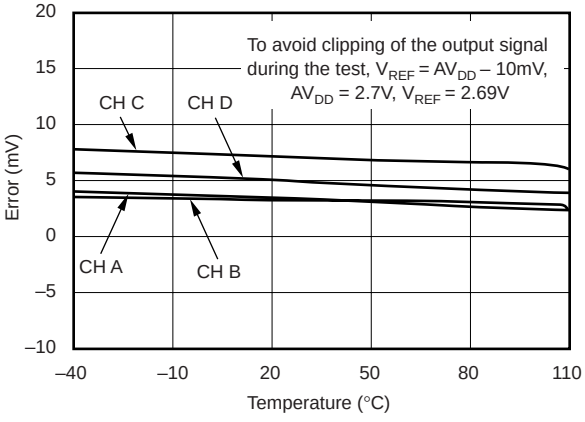
ZERO-SCALE ERROR vs TEMPERATURE



FULL-SCALE ERROR vs TEMPERATURE



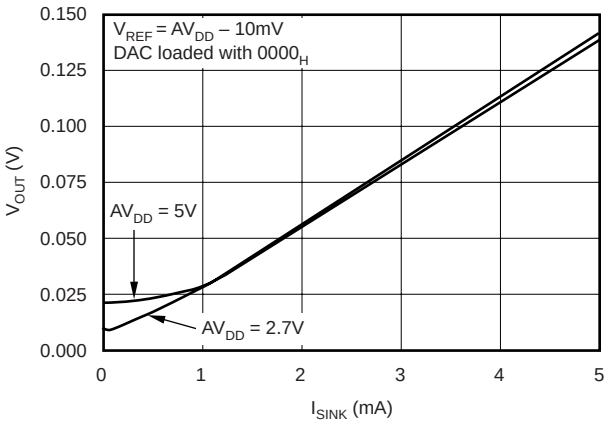
FULL-SCALE ERROR vs TEMPERATURE



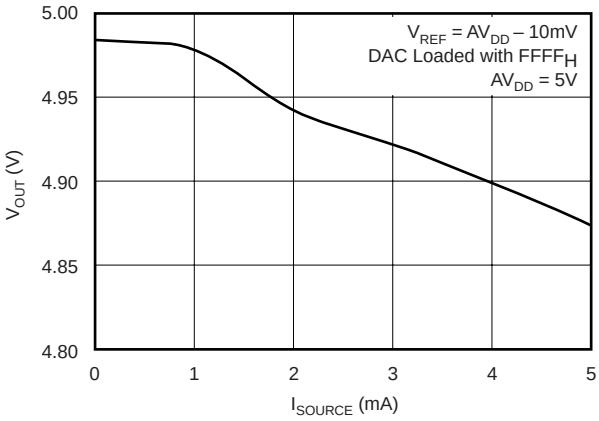
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, unless otherwise noted.

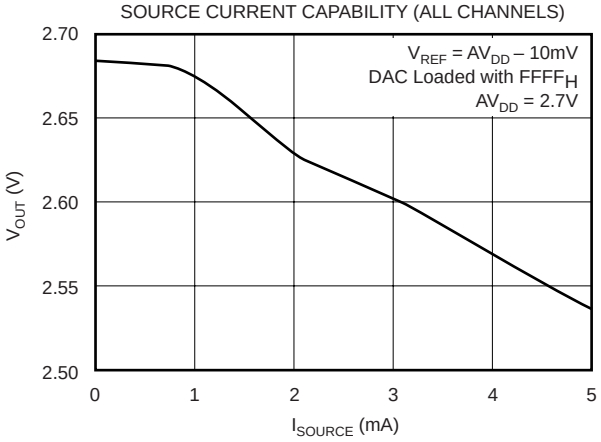
SINK CURRENT CAPABILITY (ALL CHANNELS)



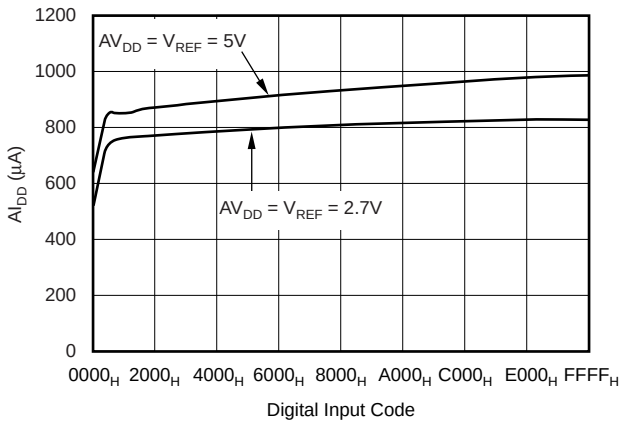
SOURCE CURRENT CAPABILITY (ALL CHANNELS)



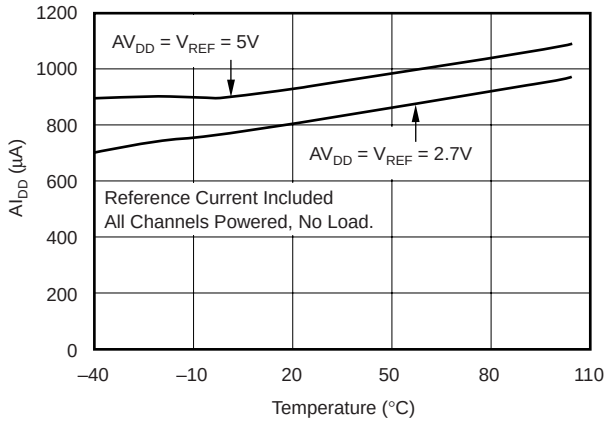
SOURCE CURRENT CAPABILITY (ALL CHANNELS)



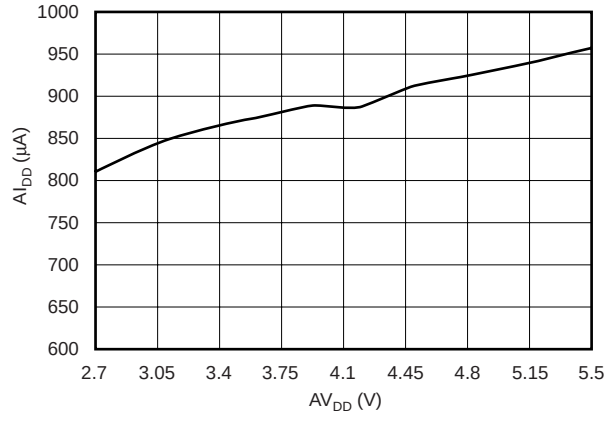
SUPPLY CURRENT vs DIGITAL INPUT CODE



SUPPLY CURRENT vs TEMPERATURE



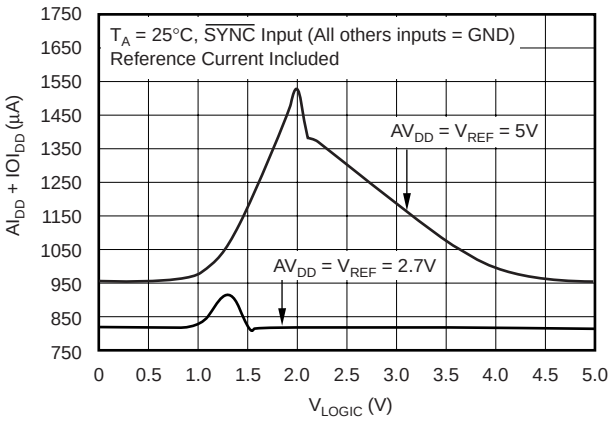
SUPPLY CURRENT vs SUPPLY VOLTAGE



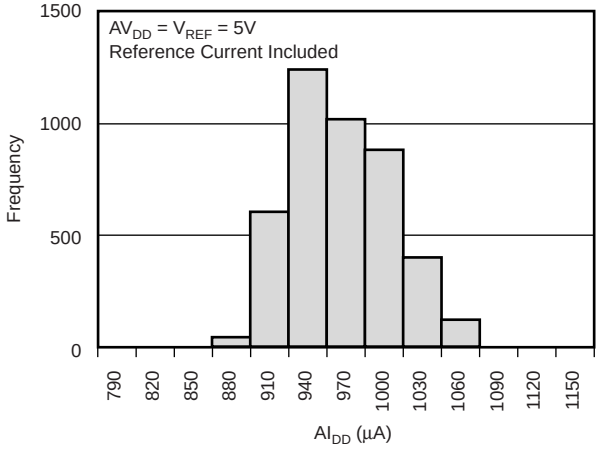
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, unless otherwise noted.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE



HISTOGRAM OF CURRENT CONSUMPTION



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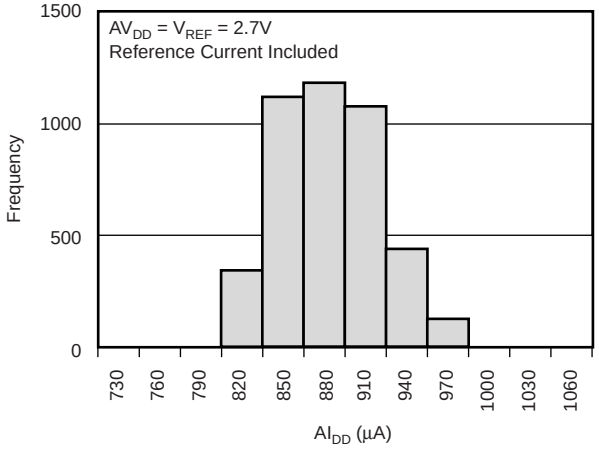
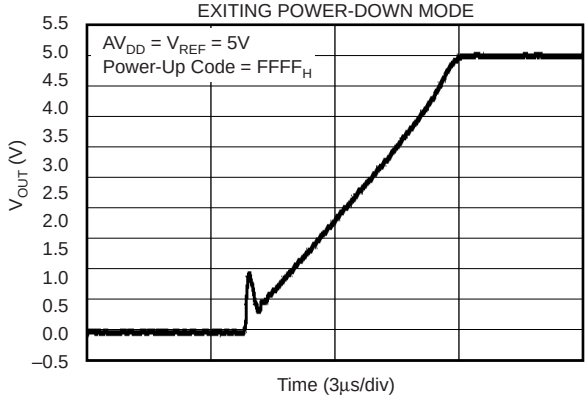
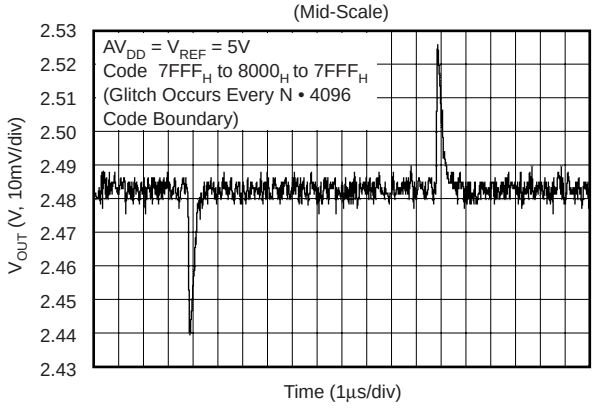


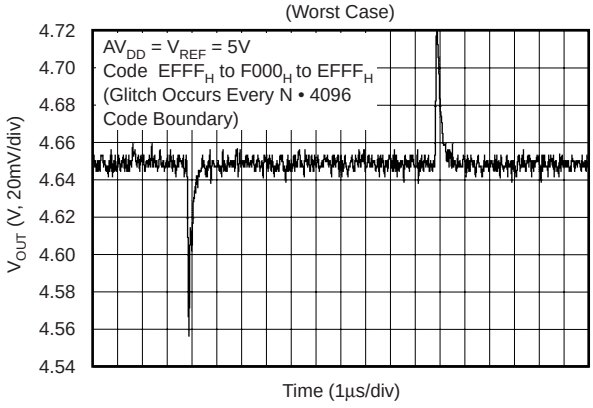
EXITING POWER-DOWN MODE



OUTPUT GLITCH
(Mid-Scale)

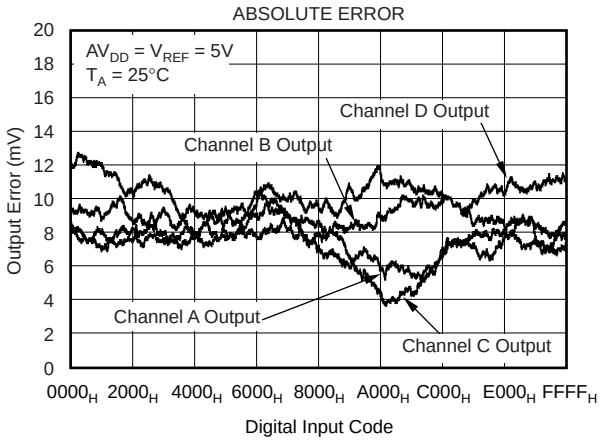


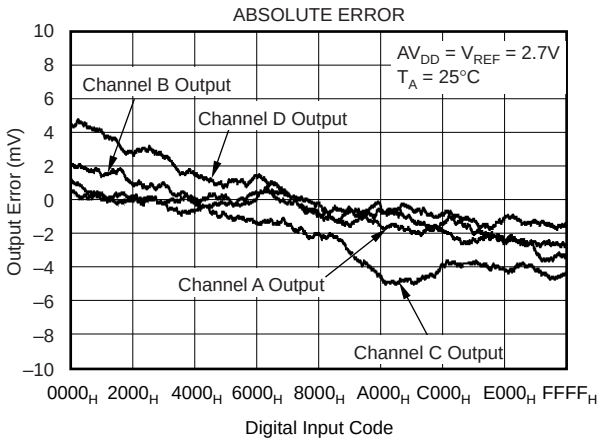
OUTPUT GLITCH
(Worst Case)

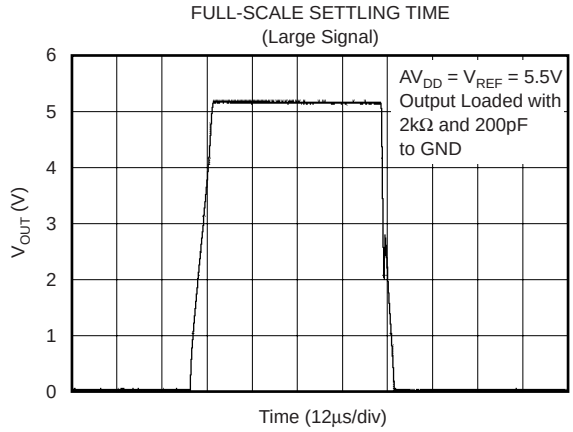


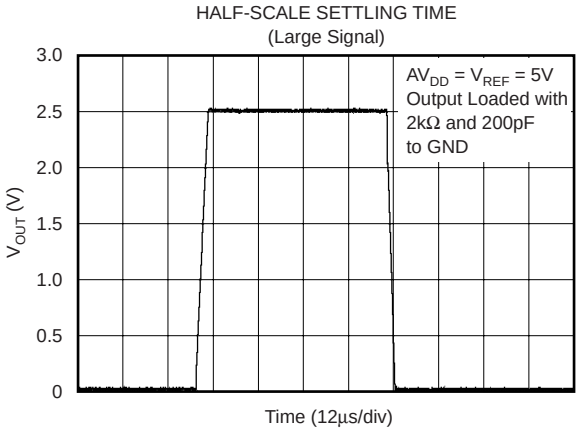
TYPICAL CHARACTERISTICS (Cont.)

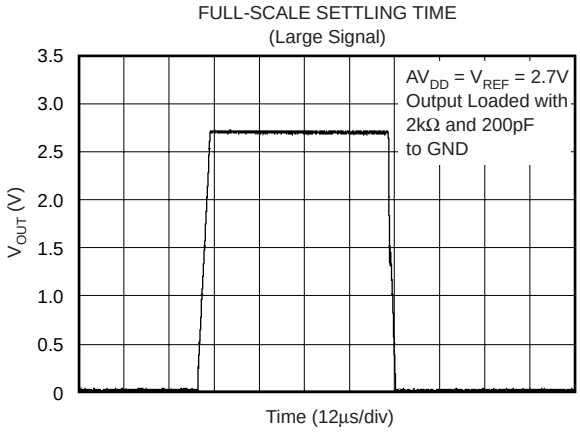
At T_A = +25°C, unless otherwise noted.

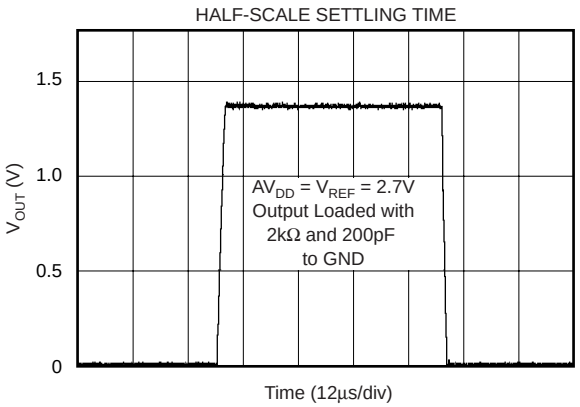








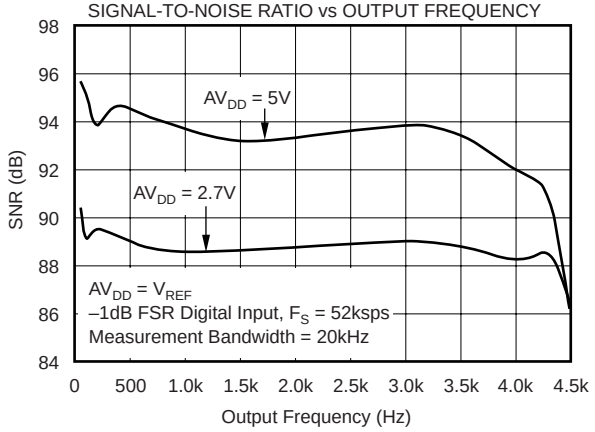




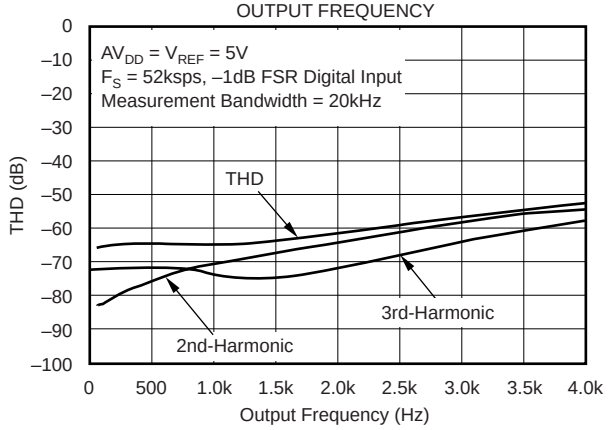
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, unless otherwise noted.

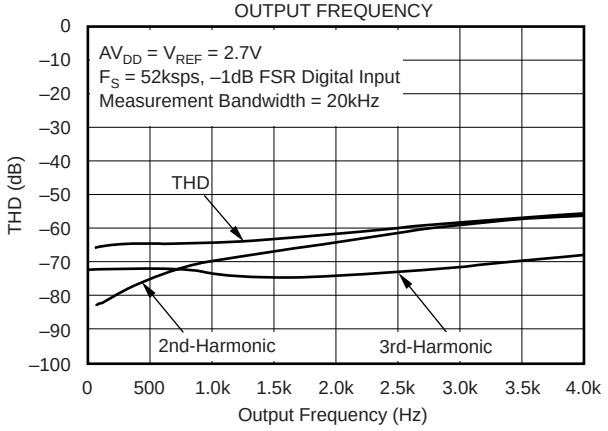
SIGNAL-TO-NOISE RATIO vs OUTPUT FREQUENCY



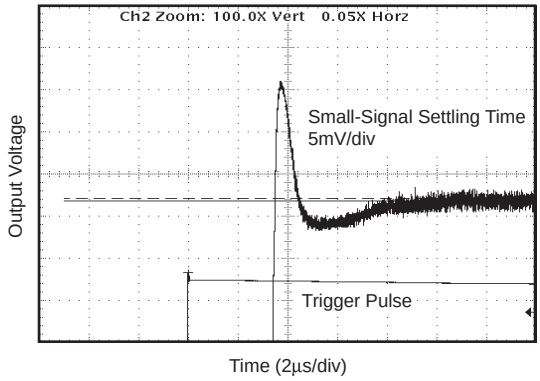
TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY



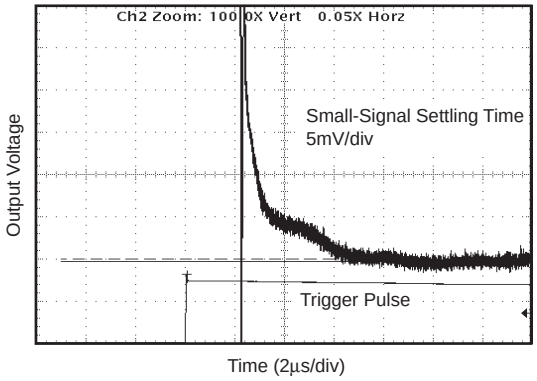
TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY



FULL-SCALE SETTLING TIME (Small-Signal-Positive Going Step)



FULL-SCALE SETTLING TIME (Small-Signal-Negative Going Step)



THEORY OF OPERATION

DAC SECTION

The architecture of each channel of the DAC8534 consists of a resistor-string DAC followed by an output buffer amplifier. Figure 1 shows a simplified block diagram of the DAC architecture.

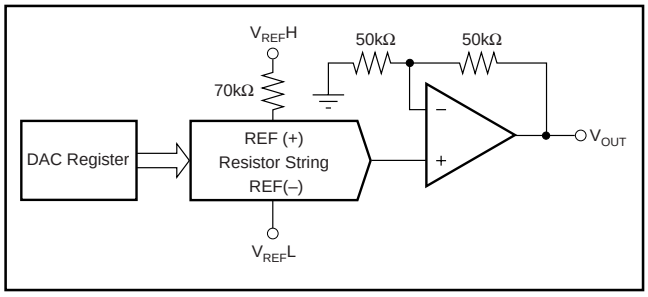


FIGURE 1. DAC8534 Architecture.

The input coding for each device is unipolar straight binary, so the ideal output voltage is given by:

$$V_{OUT}X = 2 \bullet V_{REF}L + (V_{REF}H - V_{REF}L) \bullet \frac{D_{IN}}{65536}$$

where D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 65535. $V_{OUT}X$ refers to channel A or through D.

RESISTOR STRING

The resistor string section is shown in Figure 2. It is simply a divide-by-2 resistor followed by a string of resistors. The code loaded into the DAC register determines at which node on the string the voltage is tapped off. This voltage is then applied to the output amplifier by closing one of the switches connecting the string to the amplifier.

OUTPUT AMPLIFIER

Each output buffer amplifier is capable of generating rail-to-rail voltages on its output which approaches an output range of 0V to AV_{DD} (gain and offset errors must be taken into account). Each buffer is capable of driving a load of 2kΩ in parallel with 1000pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical characteristics.

SERIAL INTERFACE

The DAC8534 uses a 3-wire serial interface ($\overline{SYNC}$, SCLK, and D_{IN}), which is compatible with SPI™, QSPI™, and Microwire™ interface standards, as well as most DSPs. See the Serial Write Operation timing diagram for an example of a typical write sequence.

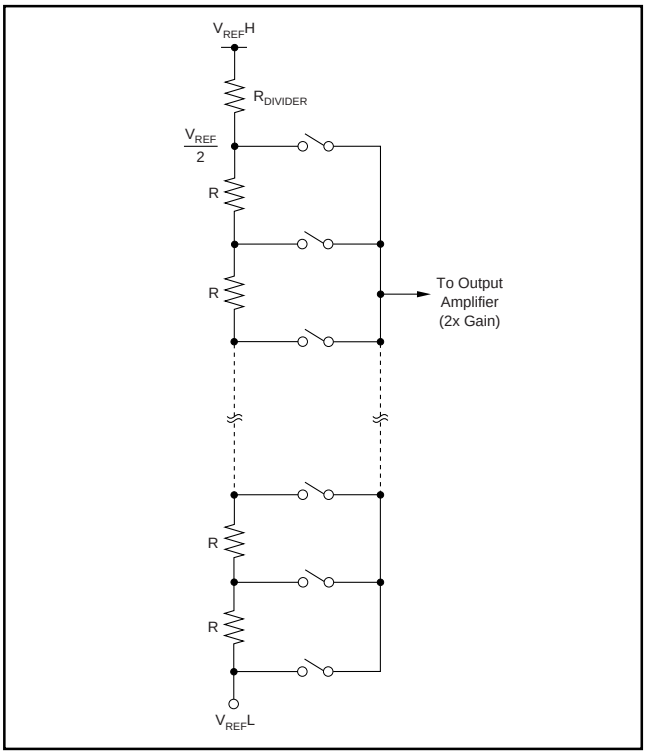


FIGURE 2. Resistor String.

The write sequence begins by bringing the $\overline{SYNC}$ line LOW. Data from the D_{IN} line is clocked into the 24-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 30MHz, making the DAC8534 compatible with high-speed DSPs. On the 24th falling edge of the serial clock, the last data bit is clocked into the shift register and the shift register gets locked. Further clocking does not change the shift register data. Once 24 bits are locked into the shift register, the 8MSBs are used as control bits and the 16LSBs are used as data. After receiving the 24th falling clock edge, DAC8534 decodes the 8 control bits and 16 data bits to perform the required function, without waiting for a $\overline{SYNC}$ rising edge. A new SPI sequence starts at the next falling edge of $\overline{SYNC}$. A rising edge of $\overline{SYNC}$ before the 24-bit sequence is complete resets the SPI interface; no data transfer occurs.

At this point, the $\overline{SYNC}$ line may be kept LOW or brought HIGH. In either case, the minimum delay time from the 24th falling SCLK edge to the next falling $\overline{SYNC}$ edge must be met in order to properly begin the next cycle. To assure the lowest power consumption of the device, care should be taken that the digital input levels are as close to each rail as possible. (Please refer to the “Typical Characteristics” section for the “Supply Current vs Logic Input Voltage” transfer characteristic curve.)

IOV_{DD} AND VOLTAGE TRANSLATORS

The IOV_{DD} pin powers the digital input structures of the DAC8534. For single-supply operation, it could be tied to AV_{DD}. For dual-supply operation, the IOV_{DD} pin provides interface flexibility with various CMOS logic families and it should be connected to the logic supply of the system. Analog circuits and internal logic of the DAC8534 use AV_{DD} as the supply voltage. The external logic high inputs get translated to AV_{DD} by level shifters. These level shifters use the IOV_{DD} voltage as a

reference to shift the incoming logic HIGH levels to AV_{DD}. IOV_{DD} is ensured to operate from 2.7V to 5.5V regardless of the AV_{DD} voltage, which ensures compatibility with various logic families. Although specified down to 2.7V, IOV_{DD} will operate at as low as 1.8V with degraded timing and temperature performance. For lowest power consumption, logic V_{IH} levels should be as close as possible to IOV_{DD}, and logic V_{IL} levels should be as close as possible to GND voltages.

INPUT SHIFT REGISTER

The input shift register (SR) of the DAC8534 is 24 bits wide, as shown in Figure 3, and is made up of 8 control bits (DB16-DB23) and 16 data bits (DB0-DB15). The first two control bits (DB22 and DB23) are the address match bits. The DAC8534 offers additional hardware-enabled addressing capability allowing a single host to talk to up to four DAC8534s through a single SPI bus without any glue logic, enabling up to 16-channel operation. The state of DB23 should match the state of pin A1; similarly, the state of DB22 should match the state of pin A0. If there is no match, the control command and the data (DB21...DB0) are ignored by the DAC8534. That is, if there is no match, the DAC8534 is not addressed. Address matching can be overridden by the broadcast update, as will be explained.

LD 1 (DB20) and LD 0 (DB21) control the updating of each analog output with the specified 16-bit data value or power-down command. Bit DB19 is a “Don’t Care” bit which does not affect the operation of the DAC8534 and can be 1 or 0. The DAC Channel Select Bits (DB17, DB18) control the destination of the data (or power-down command) from DAC A through DAC D. The final control bit, PD0 (DB16), selects the power-down mode of the DAC8534 channels.

The DAC8534 also supports a number of different load commands. The load commands include broadcast commands to address all the DAC8534s on an SPI bus. The load commands can be summarized as follows:

DB21 = 0 and DB20 = 0: Single-channel store. The temporary register (data buffer) corresponding to a DAC selected by DB18 and DB17 is updated with the contents of SR data (or power-down).

DB21 = 0 and DB20 = 1: Single-channel update. The temporary register and DAC register corresponding to a DAC selected by DB18 and DB17 are updated with the contents of SR data (or power-down).

DB21 = 1 and DB20 = 0: Simultaneous update. A channel selected by DB18 and DB17 gets updated with the SR data, and simultaneously, all the other channels get updated with previous stored data (or power-down).

DB21 = 1 and DB20 = 1: Broadcast update. All the DAC8534s on the SPI bus respond, regardless of address matching. If DB18 = 0, then SR data gets ignored, all channels from all DAC8534s get updated with previously stored data (or power-down). If DB18 = 1, then SR data (or power-down) updates all channels of all DAC8534s in the system. This broadcast update feature allows the simultaneous update of up to 16 channels.

Power-down/data selection is as follows:

DB16 is a power-down flag. If this flag is set, then DB15 and DB14 select one of the four power-down modes of the device as described in Table I. If DB16 = 1, DB15 and DB14 no longer represent the two MSBs of data, they represent a power-down condition described in Table I. Similar to data, power-down conditions can be stored at the temporary registers of each DAC. It is possible to update DACs simultaneously either with data, power-down, or a combination of both.

Please refer to Table II for more information.

PD0 (DB16)	PD1 (DB15)	PD2 (DB14)	OPERATING MODE
1	0	0	Output High Impedance
1	0	1	Output Typically 1kΩ to GND
1	1	0	Output Typically 100kΩ to GND
1	1	1	Output High Impedance

TABLE I. DAC8534 Power-Down Modes.

$\overline{\text{SYNC}}$ INTERRUPT

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept LOW for at least 24 falling edges of SCLK and the addressed DAC register is updated on the 24th falling edge. However, if $\overline{\text{SYNC}}$ is brought HIGH before the 24th falling edge, it acts as an interrupt to the write sequence; the shift register is reset and the write sequence is discarded. Neither an update of the data buffer contents, DAC register contents, nor a change in the operating mode occurs (see Figure 4).

POWER-ON RESET

The DAC8534 contains a power-on reset circuit that controls the output voltage during power-up. On power-up, the DAC registers are filled with zeros and the output voltages are set to zero-scale; they remain there until a valid write sequence and load command is made to the respective DAC channel. This is useful in applications where it is important to know the state of the output of each DAC output while the device is in the process of powering up. No device pin should be brought high before power is applied to the device.

POWER-DOWN MODES

The DAC8534 utilizes four modes of operation. These modes are accessed by setting three bits (PD2, PD1, and PD0) in the shift register and performing a “Load” action to the DACs. The DAC8534 offers a very flexible power-down interface based on channel register operation. A channel consists of a

DB23											DB12
A1	A0	LD1	LD0	X	DAC Select 1	DAC Select 0	PD0	D15	D14	D13	D12
DB11											**DB0**
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

FIGURE 3. DAC8534 Data Input Register Format.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13-D0	DESCRIPTION
A1	A0	Load 1	Load 0	Don't Care	DAC Sel 1	DAC Sel 0	PD0	MSB	MSB-1	MSB-2...LSB	
(Address Select)											
0/1	0/1	See Below									This address selects 1 of 4 possible devices on a single SPI data bus based on each device's address pin(s) state.
(A0 and A1 should correspond to the package address set via pins 13 and 14.)		0	0	X	0	0	0	Data			Write To Buffer A w/Data
		0	0	X	0	1	0	Data			Write To Buffer B w/Data
		0	0	X	1	0	0	Data			Write To Buffer C w/Data
		0	0	X	1	1	0	Data			Write To Buffer D w/Data
		0	0	X	(00, 01, 10, or 11)		1	(see Table I)		0	Write To Buffer (selected by DB17 and DB18) w/Power-Down Command
		0	1	X	(00, 01, 10, or 11)		0	Data			Write To Buffer w/Data and Load DAC (selected by DB17 and DB18)
		0	1	X	(00, 01, 10, or 11)		1	(see Table I)		0	Write To Buffer w/Power-Down Command and Load DAC (selected by DB17 and DB18)
		1	0	X	(00, 01, 10, or 11)		0	Data			Write To Buffer w/Data (selected by DB17 and DB18) and Load All DACs
		1	0	X	(00, 01, 10, or 11)		1	(see Table I)		0	Write To Buffer w/Power-Down Command (selected by DB17 and DB18) and Load All DACs
Broadcast Modes											
X	X	1	1	X	0	X	X	X			Load All DACs, All Device, and All Buffers with Stored Data
X	X	1	1	X	1	X	0	Data			Write To All Devices and Load All Dacs, with SR Data
X	X	1	1	X	1	X	1	(see Table I)		0	Write To All Devices w/Power-Down Command in SR

TABLE II. Control Matrix.

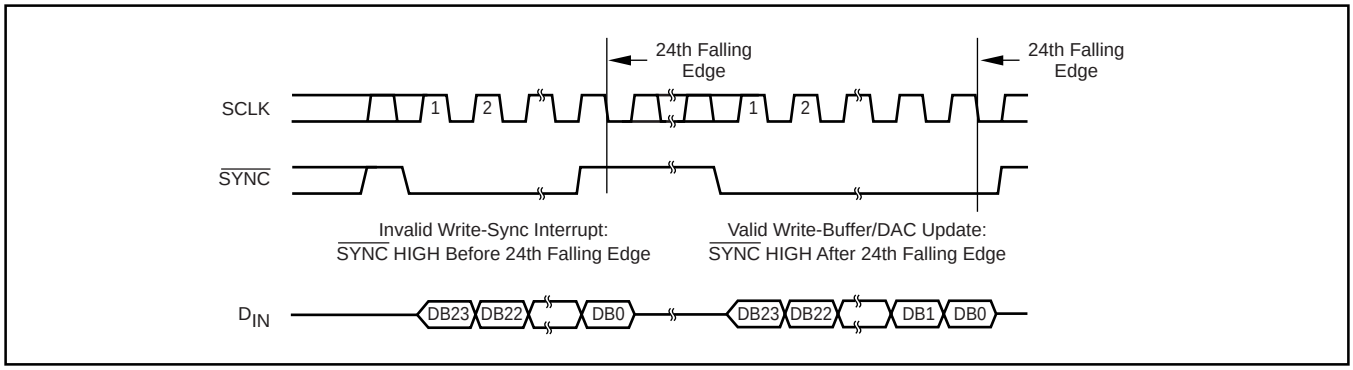


FIGURE 4. Interrupt and Valid $\overline{\text{SYNC}}$ Timing.

single 16-bit DAC with power-down circuitry, a temporary storage register (TR), and a DAC register (DR). TR and DR are both 18-bit wide. Two MSBs represent power-down condition and 16LSBs represent data for TR and DR. By adding bits 17 and 18 to TR and DR, a power-down condition can be temporarily stored and used just like data. Internal circuits ensure that DB15 and DB14 get transfered to TR17 and TR16 (DR17 and DR16), when DB16 = 1.

The DAC8534 treats the power-down condition like data and all the operational modes are still valid for power-down. It is possible to broadcast a power-down condition to all the DAC8534s in a system, or it is possible to simultaneously power-down a channel while updating data on other channels.

DB16, DB15, and DB14 = 100 represent a power-down condition with Hi-Z output impedance for a selected channel. Same is true for 111. 101 represents a power-down condition with 1k output impedance and 110 represents a power-down condition with 100k output impedance.

When both bits are set to 0 or 1, the device enters a high-impedance state with a typical power consumption of 3pA at 5V. For the two low impedance output modes, however, the supply current falls to 100nA at 5V (50nA at 3V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the device is known while it is in power-down mode. There are three different options for power-down: the output is connected internally to GND through a 1kΩ resistor, a 100kΩ resistor, or it is left open-circuited (High-Impedance). The output stage is illustrated in Figure 5.

All analog circuitry is shut down when the power-down mode is activated. Each DAC will exit power-down when PD0 is set to 0, new data is written to the Data Buffer, and the DAC channel receives a "Load" command. The time to exit power-down is typically 2.5μs for AV_{DD} = 5V and 5μs for AV_{DD} = 3V (see the Typical Characteristics).

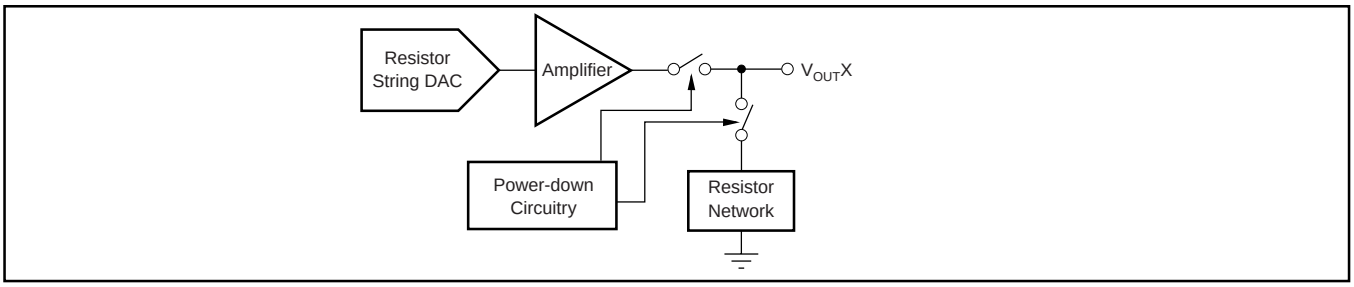


FIGURE 5. Output Stage During Power-Down (High-Impedance).

OPERATION EXAMPLES

Example 1: Write to Data Buffer A; Through Buffer D; Load DAC A Through DAC D Simultaneously

- 1st—Write to Data Buffer A:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	.....	DB1	DB0
0	0	0	0	X	0	0	0	D15	.....	D1	D0

- 2nd—Write to Data Buffer B:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	.....	DB1	DB0
0	0	0	0	X	0	1	0	D15	.....	D1	D0

- 3rd—Write to Data Buffer C:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	.....	DB1	DB0
0	0	0	0	X	1	0	0	D15	.....	D1	D0

- 4th—Write to Data Buffer D and simultaneously update all DACs:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	.....	DB1	DB0
0	0	1	0	X	1	1	0	D15	.....	D1	D0

The DAC A, DAC B, DAC C, and DAC D analog outputs simultaneously settle to the specified values upon completion of the 4th write sequence. (The “Load” command moves the digital data from the data buffer to the DAC register at which time the conversion takes place and the analog output is updated. “Completion” occurs on the 24th falling SCLK edge after $\overline{\text{SYNC}}$ LOW.)

Example 2: Load New Data to DAC A Through DAC D Sequentially

- 1st—Write to Data Buffer A and Load DAC A: DAC A output settles to specified value upon completion:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	.....	DB1	DB0
0	0	0	1	X	0	0	0	D15	.....	D1	D0

- 2nd—Write to Data Buffer B and Load DAC B: DAC B output settles to specified value upon completion:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	.....	DB1	DB0
0	0	0	1	X	0	1	0	D15	.....	D1	D0

- 3rd—Write to Data Buffer C and Load DAC C: DAC C output settles to specified value upon completion:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	.....	DB1	DB0
0	0	0	1	X	1	0	0	D15	.....	D1	D0

- 4th—Write to Data Buffer D and Load DAC D: DAC D output settles to specified value upon completion:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	.....	DB1	DB0
0	0	0	1	X	1	1	0	D15	.....	D1	D0

After completion of each write cycle, DAC analog output settles to the voltage specified.

Example 3: Power-Down DAC A and DAC B to 1kΩ and Power-Down DAC C and DAC D to 100kΩ Simultaneously

- Write power-down command to Data Buffer A: DAC A to 1kΩ.

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	.....
0	0	0	0	X	0	0	1	0	1	X	.....

• Write power-down command to Data Buffer B: DAC B to 1kΩ.

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	.....
0	0	0	0	X	0	1	1	0	1	X	.....

• Write power-down command to Data Buffer C: DAC C to 100kΩ.

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	.....
0	0	0	0	X	1	0	1	1	0	X	.....

• Write power-down command to Data Buffer D: DAC D to 100kΩ and Simultaneously Update all DACs.

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	.....
0	0	1	0	X	1	1	1	1	0	X	.....

The DAC A, DAC B, DAC C, and DAC D analog outputs simultaneously power-down to each respective specified mode upon completion of the 4th write sequence.

Example 4: Power-Down DAC A Through DAC D to High-Impedance Sequentially:

• Write power-down command to Data Buffer A and Load DAC A: DAC A output = High-Z:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	.....
0	0	0	1	X	0	0	1	1	1	X	.....

• Write power-down command to Data Buffer B and Load DAC B: DAC B output = High-Z:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	.....
0	0	0	1	X	0	1	1	1	1	X	.....

• Write power-down command to Data Buffer C and Load DAC C: DAC C output = High-Z:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	.....
0	0	0	1	X	1	0	1	1	1	X	.....

• Write power-down command to Data Buffer D and Load DAC D: DAC D output = High-Z:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	.....
0	0	0	1	X	1	1	1	1	1	X	.....

The DAC A, DAC B, DAC C, and DAC D analog outputs sequentially power-down to high-impedance upon completion of the 1st, 2nd, 3rd, and 4th write sequences, respectively.

LDAC FUNCTIONALITY

The DAC8534 offers both a software and hardware simultaneous update function. The DAC8534 double-buffered architecture has been designed so that new data can be entered for each DAC without disturbing the analog outputs. The software simultaneous update capability is controlled by the Load 1 (LD1) and Load 0 (LD0) control bits. By setting Load 1 equal to “1” all of the DAC registers will be updated on the falling edge of the 24th clock signal. When the new data has been entered into the device, all of the DAC outputs can be updated simultaneously and synchronously with the clock.

The internal DAC register is edge triggered and not level triggered, therefore, when the LDAC pin signal is transitioned from LOW to HIGH, the digital word currently in the DAC input register is latched. Additionally, it allows the DAC input registers to be written to at any point; then, the DAC output voltages can be asynchronously changed via the LDAC pin. The LDAC trigger should only be used after the buffers are properly updated through software. If DAC outputs are desired to be updated through software only, the LDAC pin must be tied low permanently.

MICROPROCESSOR INTERFACING

DAC8534 to 8051 INTERFACE

See Figure 6 for a serial interface between the DAC8534 and a typical 8051-type microcontroller. The setup for the interface is as follows: TXD of the 8051 drives SCLK of the DAC8534, while RXD drives the serial data line of the device. The $\overline{\text{SYNC}}$ signal is derived from a bit-programmable pin on the port of the 8051. In this case, port line P3.3 is used. When data is to be transmitted to the DAC8534, P3.3 is taken LOW. The 8051 transmits data in 8-bit bytes; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left LOW after the first eight bits are transmitted, then a second and third write cycle is initiated to transmit the remaining data. P3.3 is taken HIGH following the completion of the third write cycle. The 8051 outputs the serial data in a format which presents the LSB first, while the DAC8534 requires its data with the MSB as the first bit received. The 8051 transmit routine must therefore take this into account, and “mirror” the data as needed.

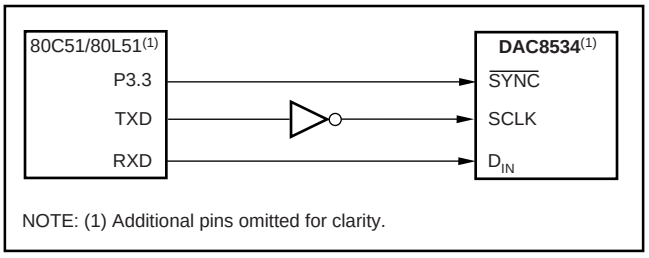


FIGURE 6. DAC8534 to 80C51/80L51 Interface.

DAC8534 to Microwire INTERFACE

Figure 7 shows an interface between the DAC8534 and any Microwire compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the DAC8534 on the rising edge of the CK signal.

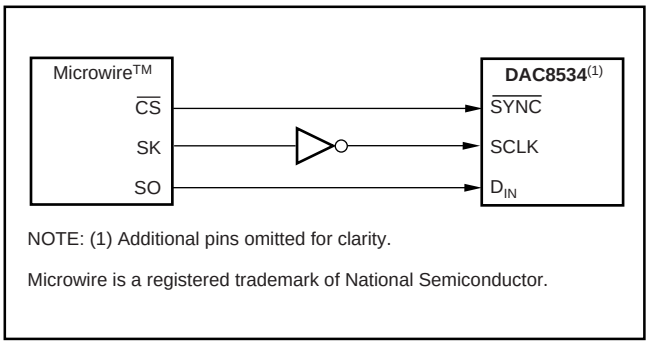


FIGURE 7. DAC8534 to Microwire Interface.

DAC8534 to 68HC11 INTERFACE

Figure 8 shows a serial interface between the DAC8534 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC8534, while the MOSI output drives the serial data line of the DAC. The $\overline{SYNC}$ signal is derived from a port line (PC7), similar to the 8051 diagram.

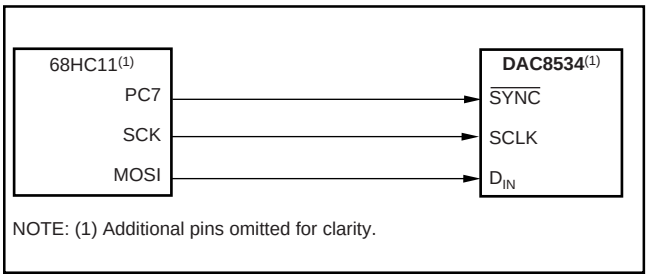


FIGURE 8. DAC8534 to 68HC11 Interface.

The 68HC11 should be configured so that its CPOL bit is 0 and its CPHA bit is 1. This configuration causes data appearing on the MOSI output to be valid on the falling edge of SCLK. When data is being transmitted to the DAC, the $\overline{SYNC}$ line is held LOW (PC7). Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. (Data is transmitted MSB first.) In order to load data to the DAC8534, PC7 is left LOW after the first eight bits are transferred, then a second and third serial write operation is performed to the DAC. PC7 is taken HIGH at the end of this procedure.

DAC8534 to TMS320 DSP INTERFACE

Figure 9 shows the connections between the DAC8534 and a TMS320 Digital Signal Processor (DSP). A Single DSP can control up to four DAC8534s without any interface logic.

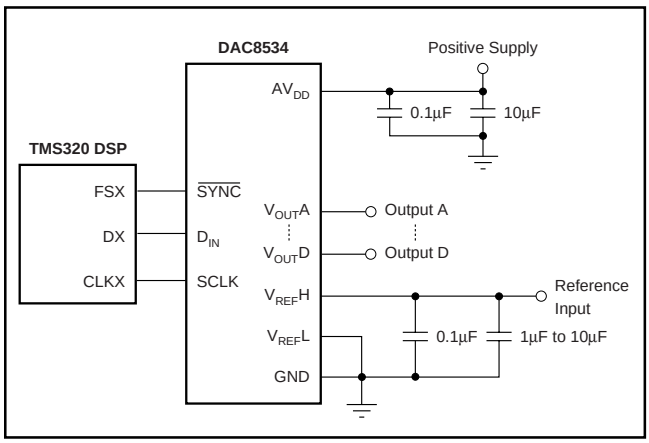


FIGURE 9. DAC8534 to TMS320 DSP.

APPLICATIONS

CURRENT CONSUMPTION

The DAC8534 typically consumes 250µA at AV_{DD} = 5V and 225µA at AV_{DD} = 3V for each active channel, including reference current consumption. Additional current consumption can occur at the digital inputs if V_{IH} << IOV_{DD}. For most efficient power operation, CMOS logic levels are recommended at the digital inputs to the DAC.

In power-down mode, typical current consumption is 200nA per channel. A delay time of 10ms to 20ms after a power-down command is issued to the DAC is typically sufficient for the power-down current to drop below 10µA.

DRIVING RESISTIVE AND CAPACITIVE LOADS

The DAC8534 output stage is capable of driving loads of up to 1000pF while remaining stable. Within the offset and gain error margins, the DAC8534 can operate rail-to-rail when driving a capacitive load. Resistive loads of 2kΩ can be driven by the DAC8534 while achieving a typical load regulation of 1%. As the load resistance drops below 2kΩ, the load regulation error increases. When the outputs of the DAC are driven to the positive rail under resistive loading, the PMOS transistor of each Class-AB output stage can enter into the linear region. When this occurs, the added IR voltage drop deteriorates the linearity performance of the DAC. This only occurs within approximately the top 20mV of the DAC's output voltage characteristic. The reference voltage applied to the DAC8534 may be reduced below the supply voltage applied to AV_{DD} in order to eliminate this condition if good linearity is a requirement at full-scale (under resistive loading conditions).

CROSSTALK AND AC PERFORMANCE

The DAC8534 architecture uses separate resistor strings for each DAC channel in order to achieve ultra-low crosstalk performance. DC crosstalk seen at one channel during a full-

scale change on the neighboring channel is typically less than 0.5LSBs. The AC crosstalk measured (for a full-scale, 1kHz sine wave output generated at one channel, and measured at the remaining output channel) is typically under –100dB.

In addition, the DAC8534 can achieve typical AC performance of 96dB SNR (Signal-to-Noise Ratio) and 65dB THD (Total Harmonic Distortion), making the DAC8534 a solid choice for applications requiring high SNR at output frequencies at or below 4kHz.

OUTPUT VOLTAGE STABILITY

The DAC8534 exhibits excellent temperature stability of 5ppm/°C typical output voltage drift over the specified temperature range of the device. This enables the output voltage of each channel to stay within a ±25µV window for a ±1°C ambient temperature change.

Good Power-Supply Rejection Ratio (PSRR) performance reduces supply noise present on AV_{DD} from appearing at the outputs to well below 10µV-s. Combined with good DC noise performance and true 16-bit differential linearity, the DAC8534 becomes a perfect choice for closed-loop control applications.

SETTLING TIME AND OUTPUT GLITCH PERFORMANCE

Settling time to within the 16-bit accurate range of the DAC8534 is achievable within 10µs for a full-scale code change at the input. Worst-case settling times between consecutive code changes is typically less than 2µs, enabling update rates up to 500ksps for digital input signals changing code-to-code. The high-speed serial interface of the DAC8534 is designed in order to support these high update rates.

For full-scale output swings, the output stage of each DAC8534 channel typically exhibits less than 100mV of overshoot and undershoot when driving a 200pF capacitive load. Code-to-code change glitches are extremely low given that the code-to-code transition does not cross an Nx4096 code boundary. Due to internal segmentation of the DAC8534, code-to-code glitches occur at each crossing of an Nx4096 code boundary. These glitches can approach 100nVs for N = 15, but settle out within ~2µs.

USING THE REF02 AS A POWER SUPPLY FOR THE DAC8534

Due to the extremely low supply current required by the DAC8534, a possible configuration is to use a REF02 +5V precision voltage reference to supply the required voltage to the DAC8534's supply input as well as the reference input, as shown in Figure 10. This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5V. The REF02 will output a steady supply voltage for the DAC8534. If the REF02 is used, the current it needs to supply to the DAC8534 is 1.085mA typical and 1.78mA max for AV_{DD} = 5V. When a DAC output is loaded, the REF02 also needs to supply the current to the load. The total typical current required (with a 5kΩ load on a given DAC output) is:

$$1.085mA + (5V/5k\Omega) = 2.085mA$$

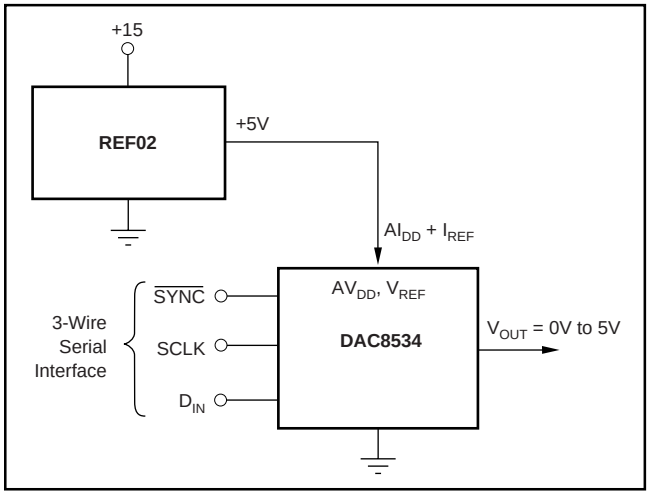


FIGURE 10. REF02 as a Power Supply to the DAC8534.

BIPOLAR OPERATION USING THE DAC8534

The DAC8534 has been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 11. The circuit shown will give an output voltage range of $\pm V_{REF}$. Rail-to-rail operation at the amplifier output is achievable using an amplifier such as the OPA703, as shown in Figure 11.

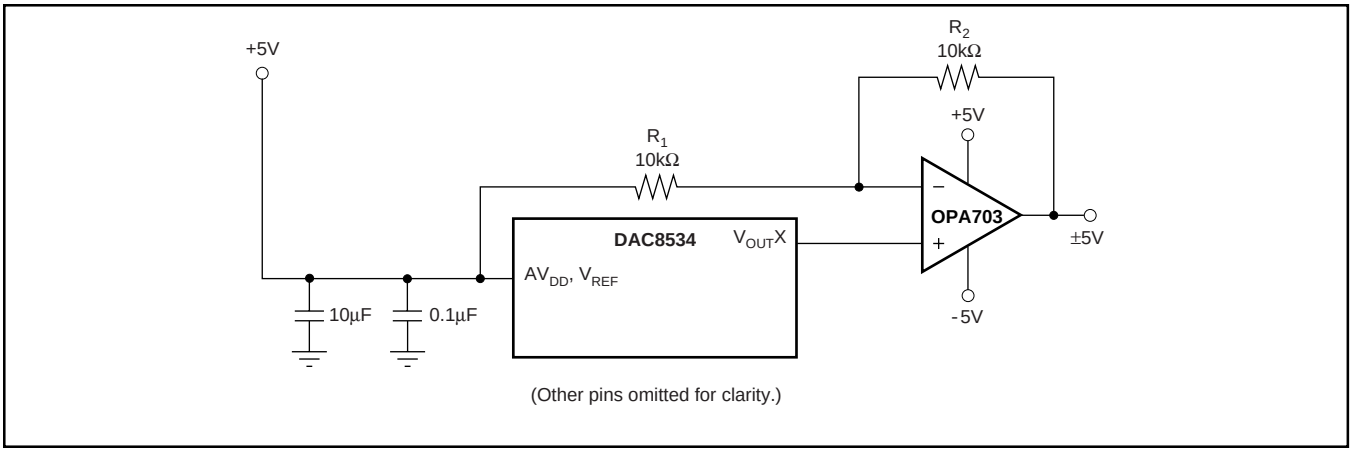


FIGURE 11. Bipolar Operation with the DAC8534.

The output voltage for any input code can be calculated as follows:

$$V_{OUT}X = \left[V_{REF} \bullet \left(\frac{D}{65536} \right) \bullet \left(\frac{R_1 + R_2}{R_1} \right) - V_{REF} \bullet \left(\frac{R_2}{R_1} \right) \right]$$

where D represents the input code in decimal (0–65535).

With V_{REF} = 5V, $R_1 = R_2$ = 10kΩ:

$$V_{OUT}X = \left(\frac{10 \bullet D}{65536} \right) - 5V$$

This is an output voltage range of ±5V with 0000_H corresponding to a –5V output and $FFFF_H$ corresponding to a +5V output. Similarly, using V_{REF} = 2.5V, a ±2.5V output voltage range can be achieved.

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The DAC8534 offers single-supply operation, and it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it will be to keep digital noise from appearing at the output.

Due to the single ground pin of the DAC8534, all return currents, including digital and analog return currents for the DAC, must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power-entry point of the system.

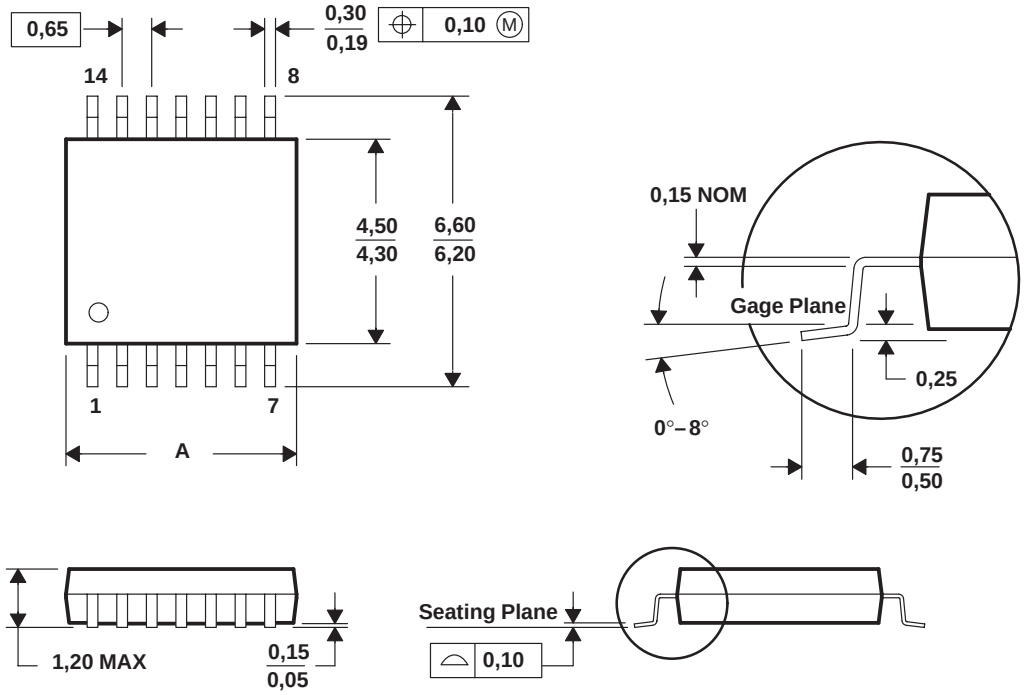
The power applied to AV_{DD} should be well regulated and low noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection, AV_{DD} should be connected to a positive power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, a 1µF to 10µF capacitor in parallel with a 0.1µF bypass capacitor is strongly recommended. In some situations, additional bypassing may be required, such as a 100µF electrolytic capacitor or even a “Pi” filter made up of inductors and capacitors—all designed to essentially low-pass filter the supply, removing the high-frequency noise.

Up to four DAC8534 devices can be used on a single SPI bus without any glue logic to create a high channel count solution. Special attention is required to avoid digital signal integrity problems when using multiple DAC8534s on the same SPI bus. Signal integrity of $\overline{SYNC}$, SCLK, and D_{IN} lines will not be an issue as long as the rise times of these digital signals are longer than six times the propagation delay between any two DAC8534 devices. Propagation speed is approximately six inches/ns on standard PCBs. Therefore, if the digital signal risetime is 1ns, the distance between any two DAC8534 devices is recommended not to exceed 1 inch. If the DAC8534s have to be further apart on the PCB, the signal rise times should be reduced by placing series resistors at the drivers for $\overline{SYNC}$, SCLK, and D_{IN} lines. If the largest distance between any two DAC8534s has to be six inches, the risetime should be reduced to 6ns with an RC network formed by the series resistor at the digital driver and the total trace and input capacitance on the PCB.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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